

GA-AX370M-GAMING 3

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PAGE	TITLE
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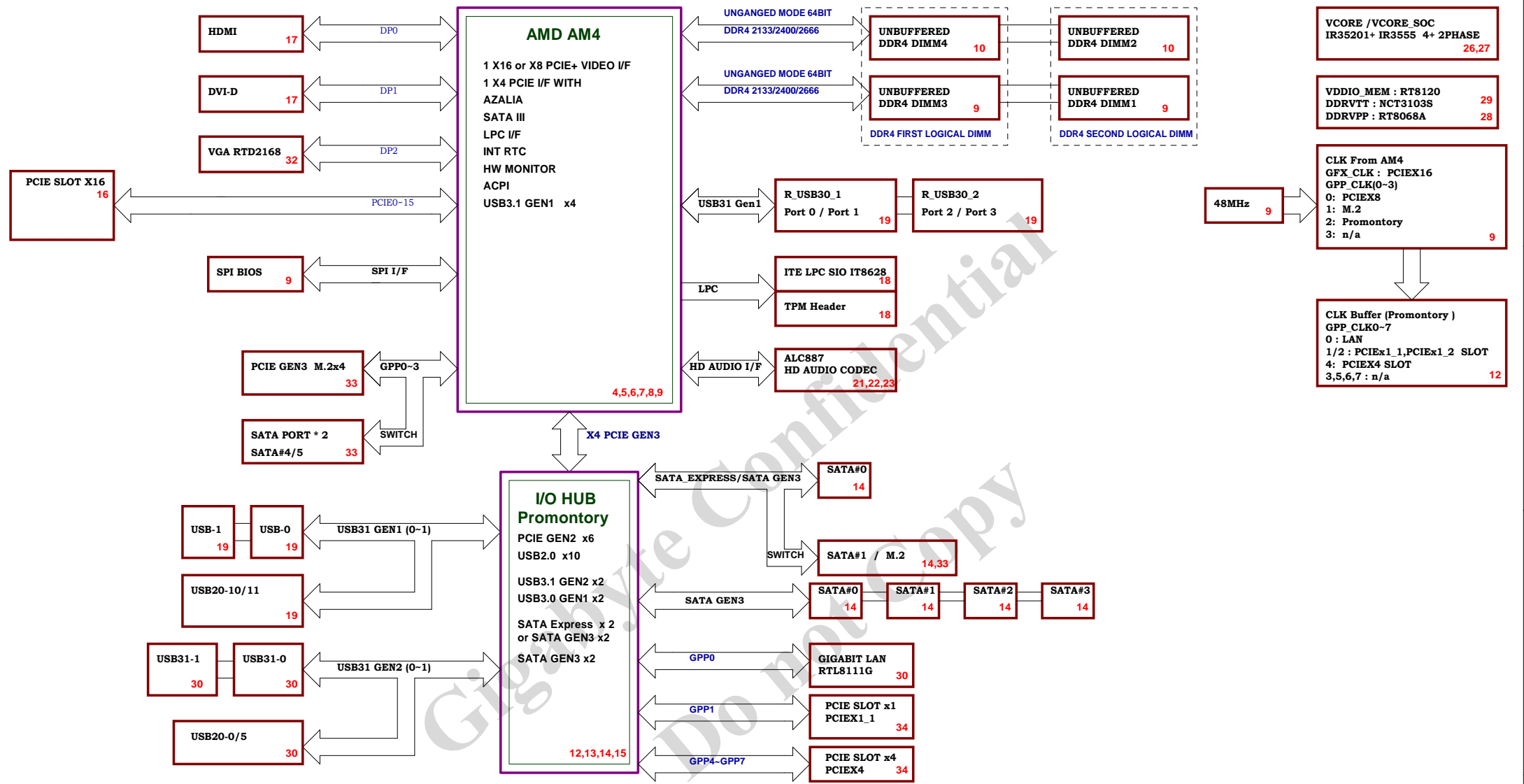
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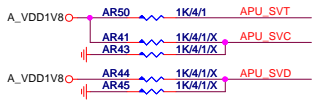
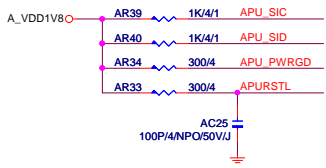
Circuit or PCB layout change for next version

Version: 1.01

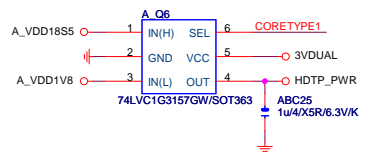
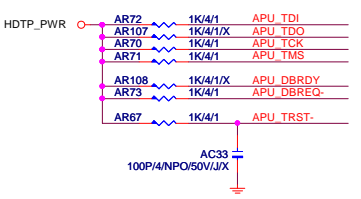
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Title BOM & PCB HISTORY			
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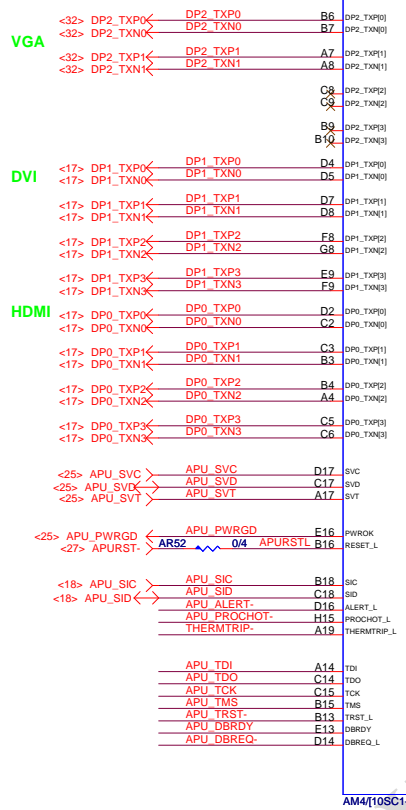
SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



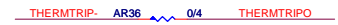
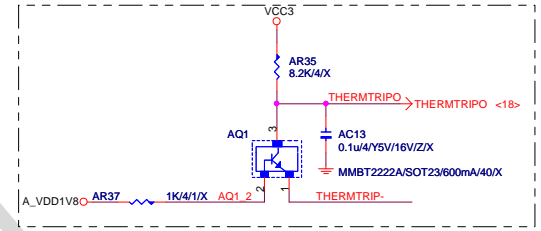
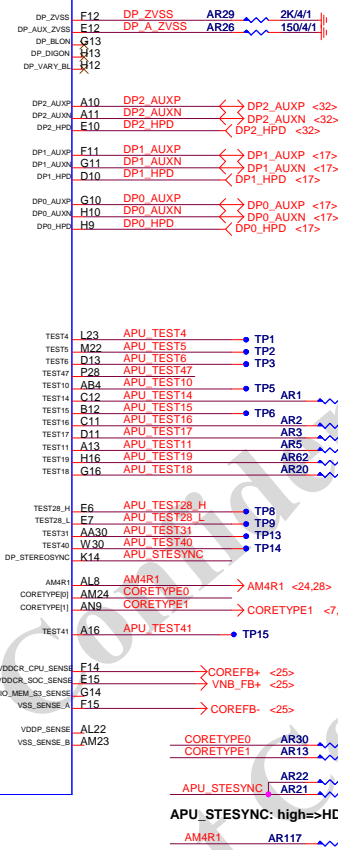
VGA

DVI

HDMI

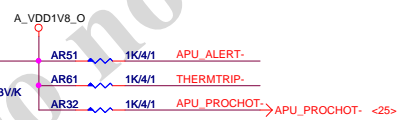
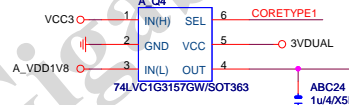


Placed within 1500 mils from APU



AM4[10SC1-P01331-11R]

A Q4

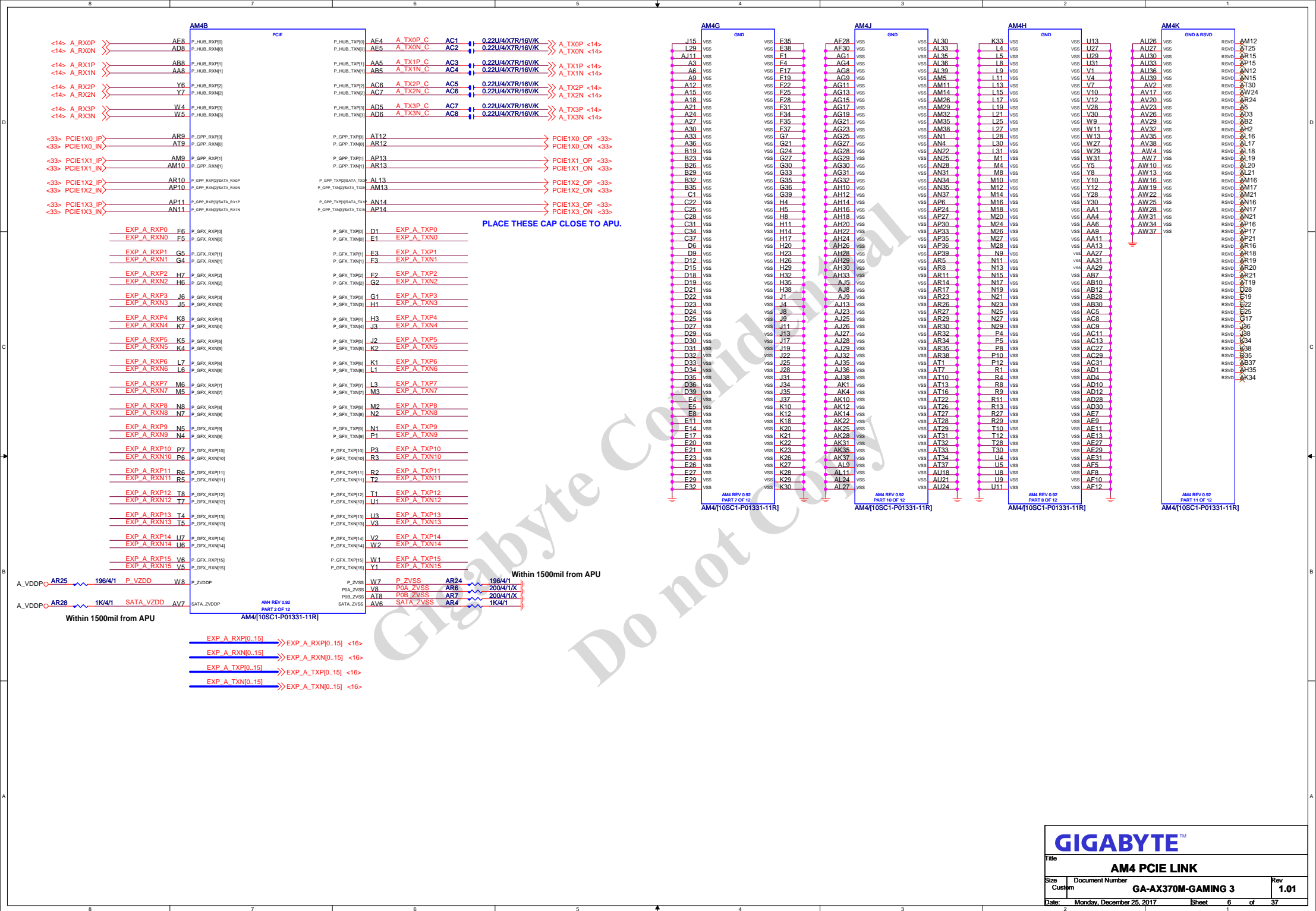


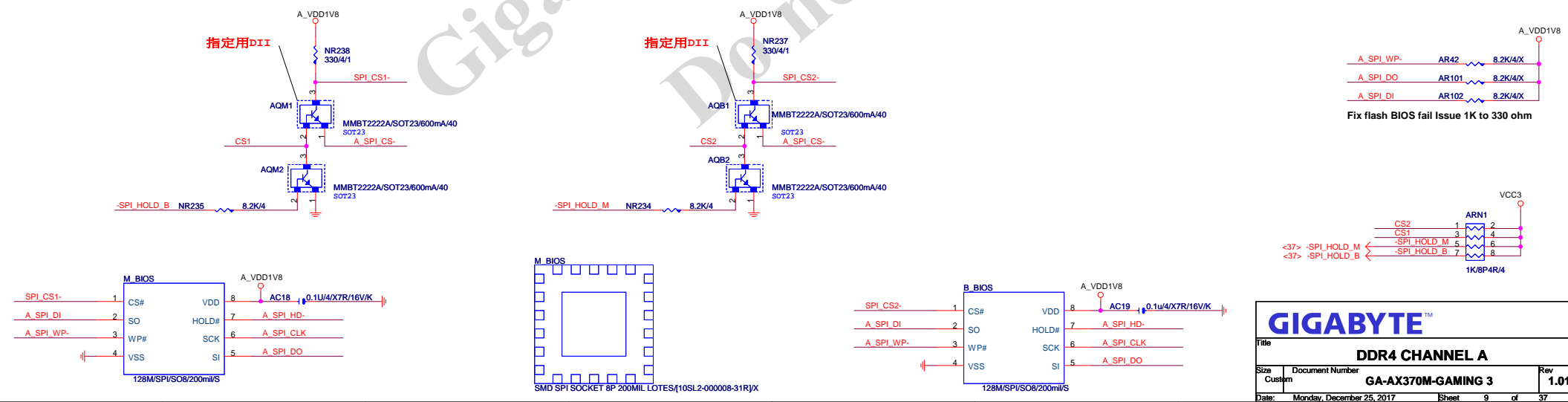
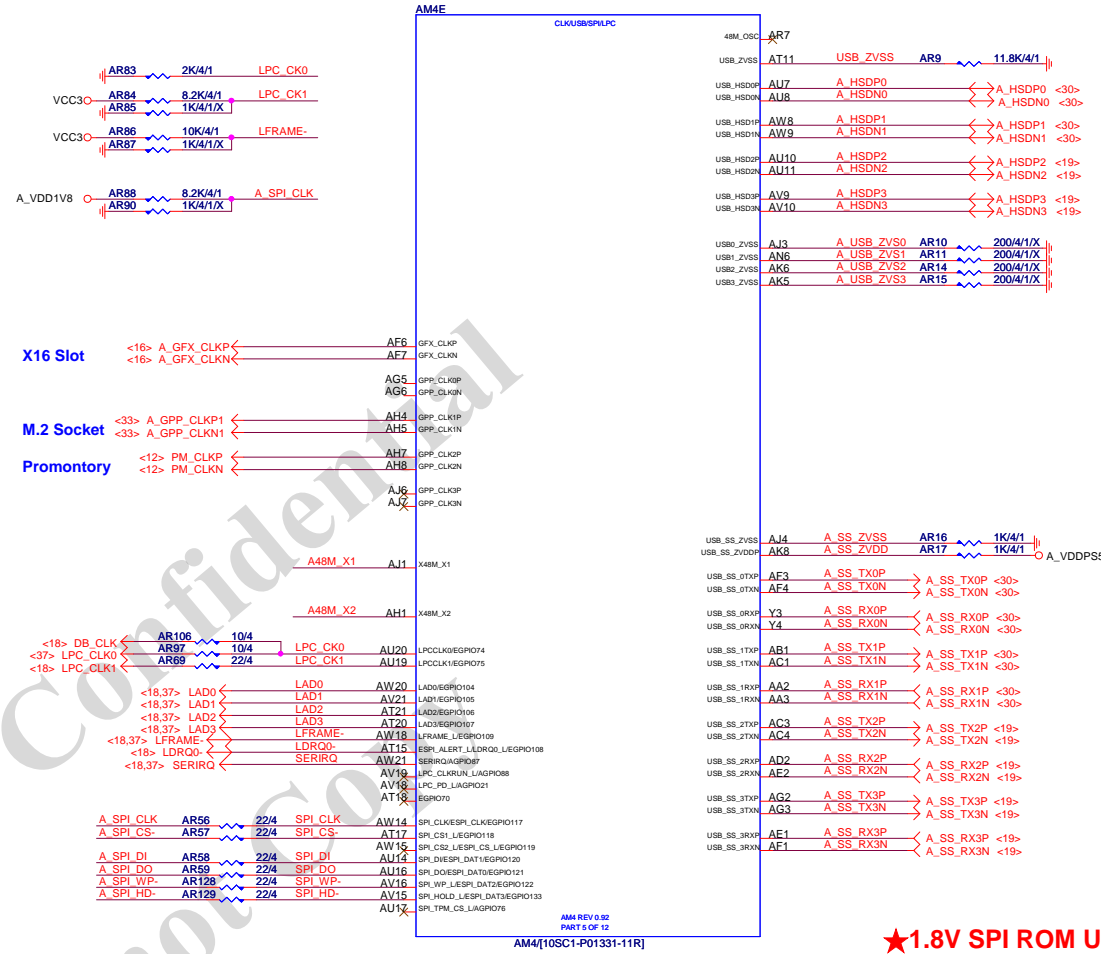
AM4 CPU CoreType

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh	TYPE 3

GIGABYTE™

Title			CPU CONTROL		
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GIGABYTETM

Title

DDR4 CHANNEL A

Size

Custom

Document Number

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Rev

1.01

Date

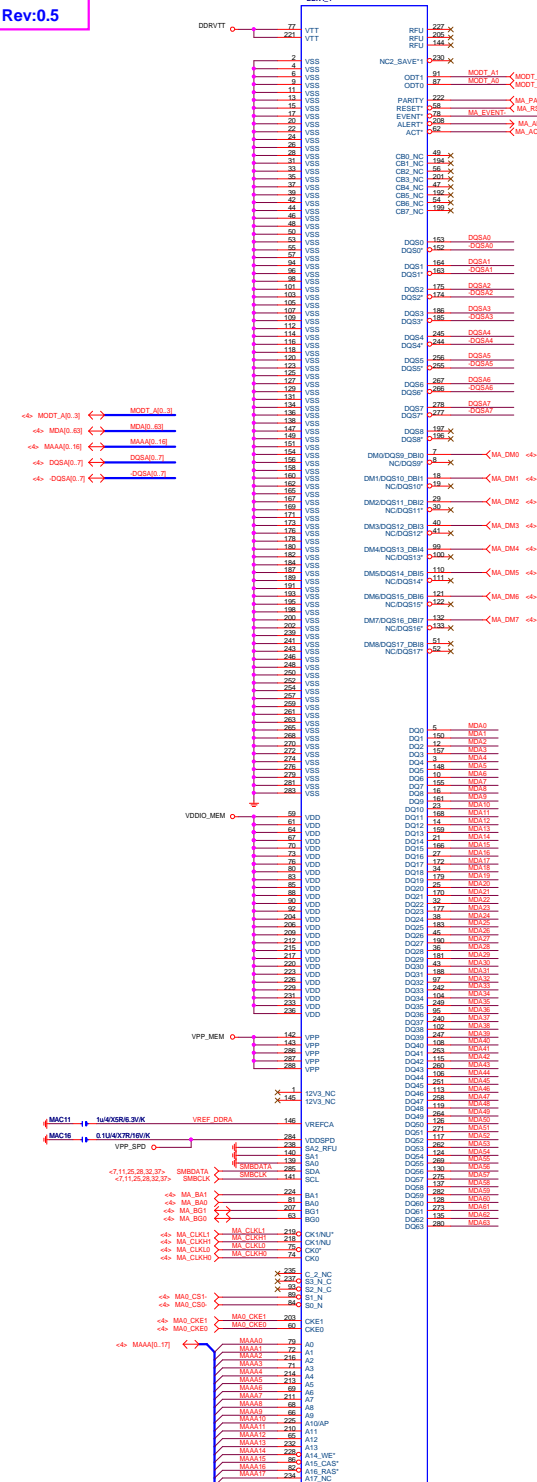
Monday, December 25, 2017

Sheet

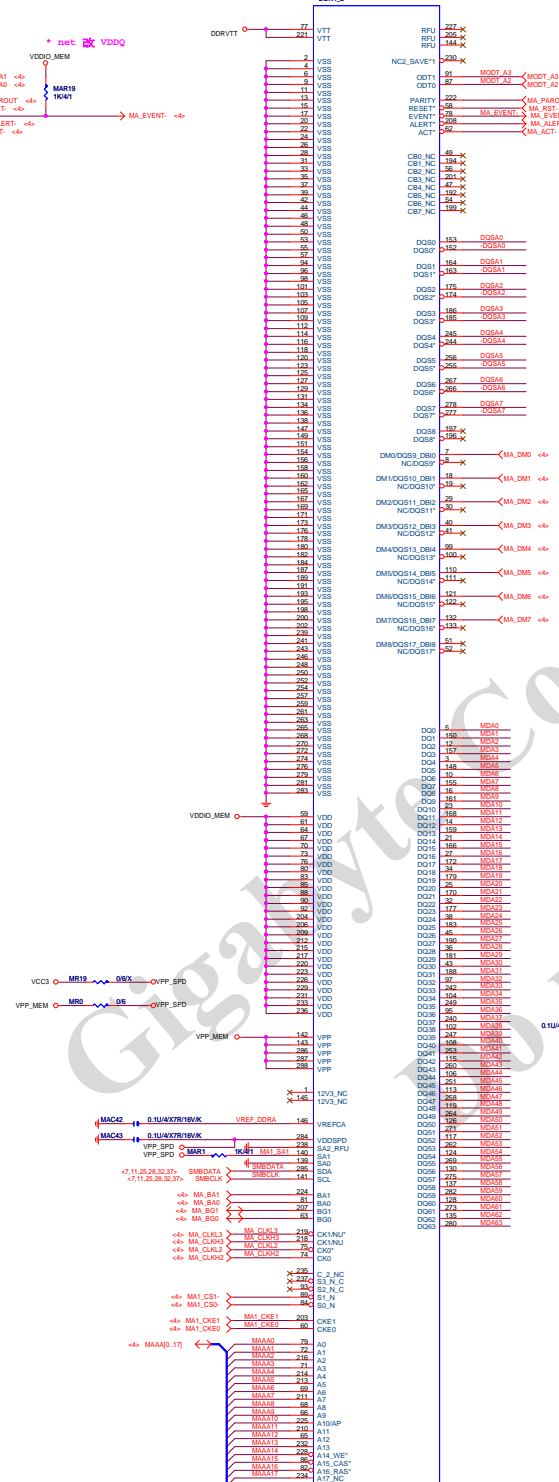
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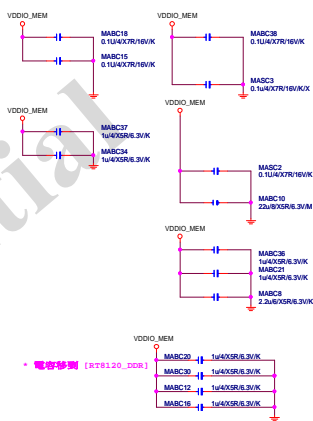
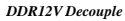
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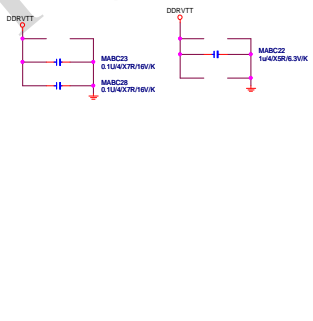
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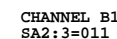
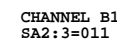


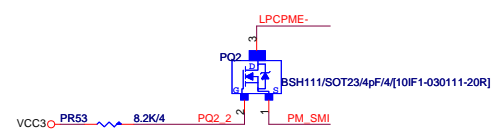
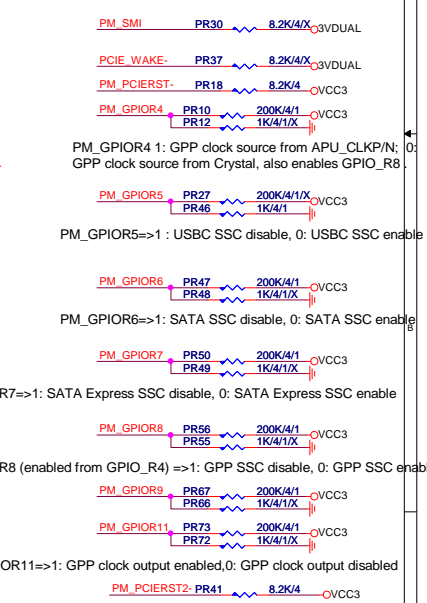
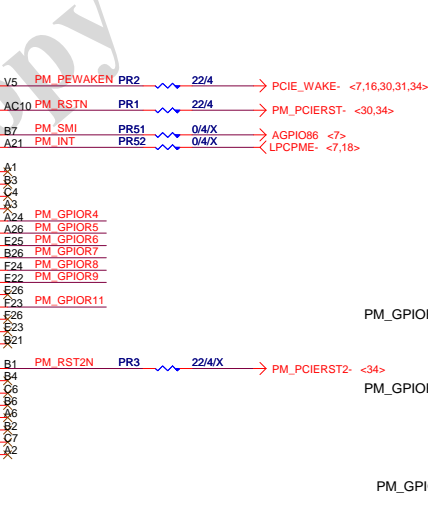
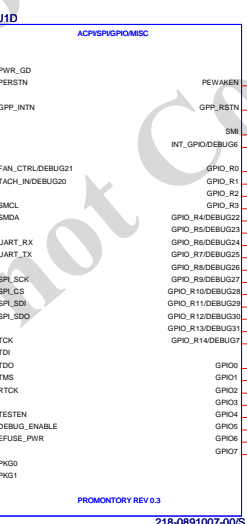
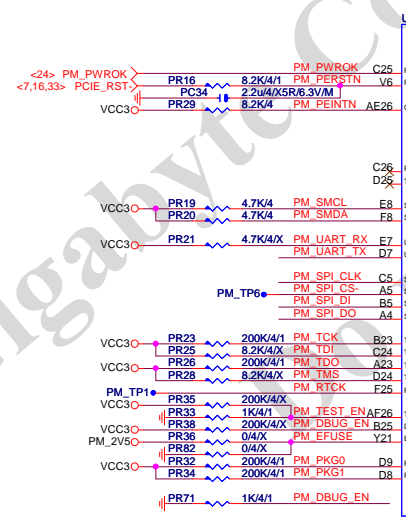
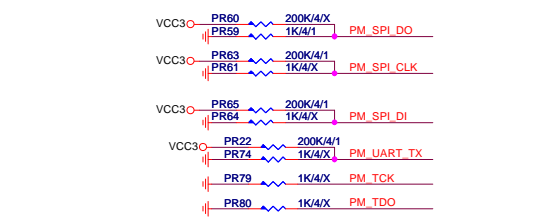
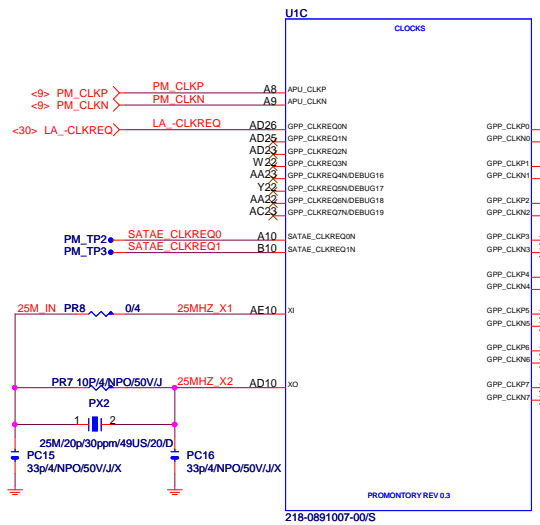
CHANNEL A1
SA2:2=010

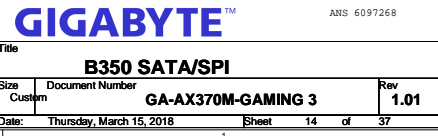


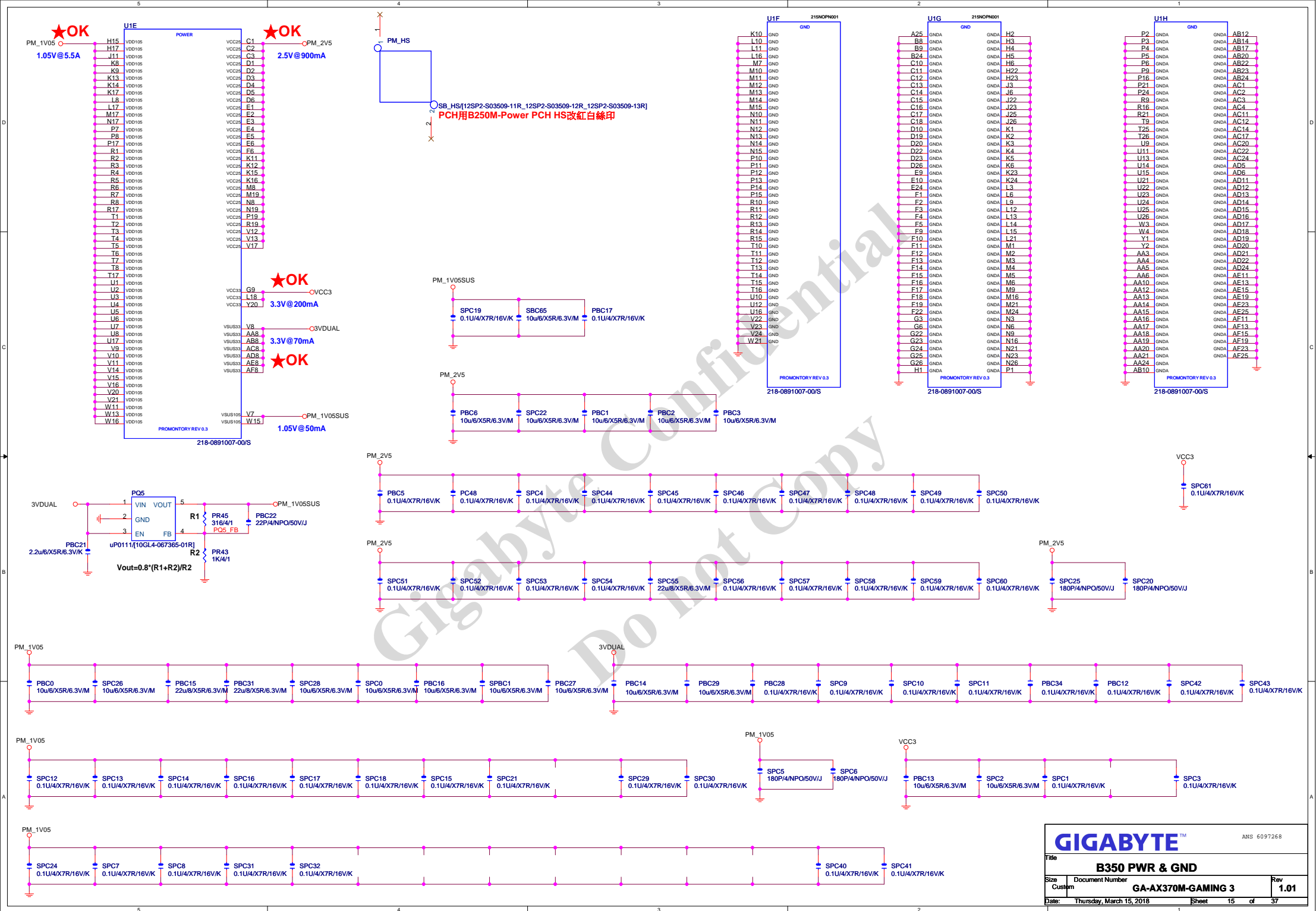
DDRVTT Decouple

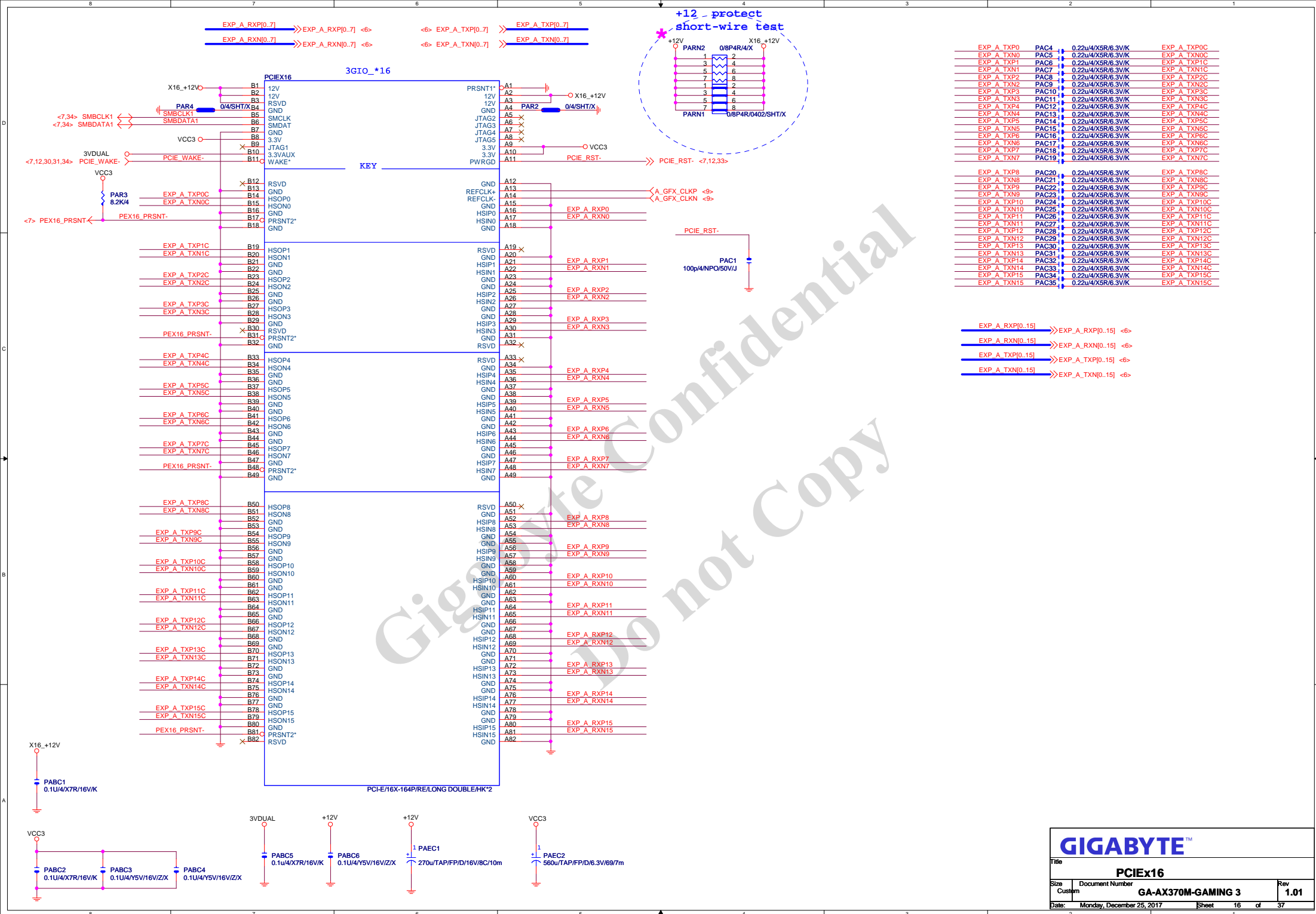


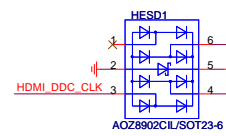
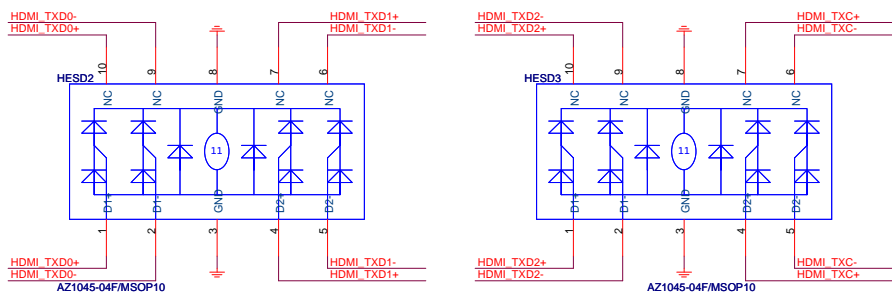
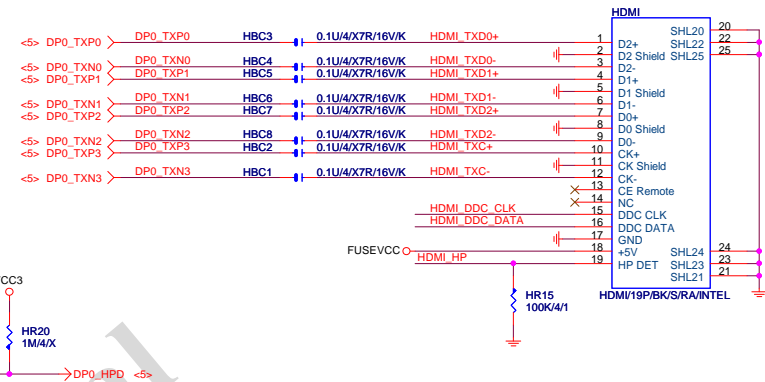
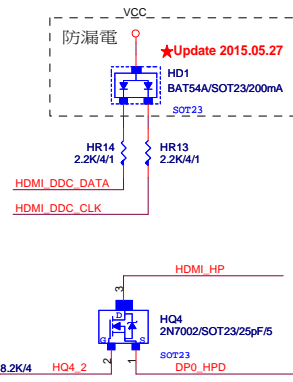
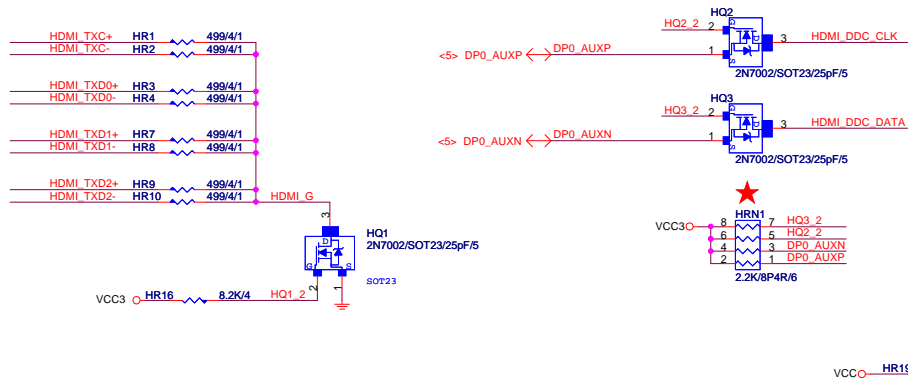








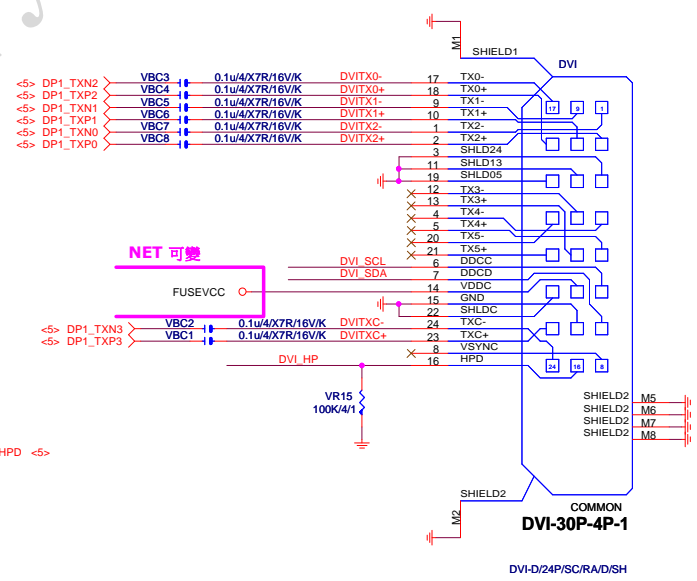
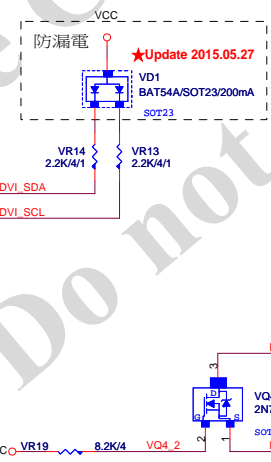
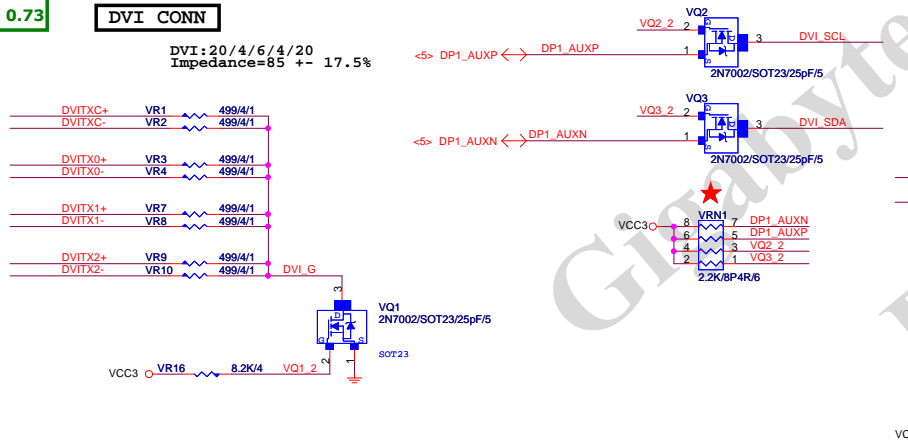




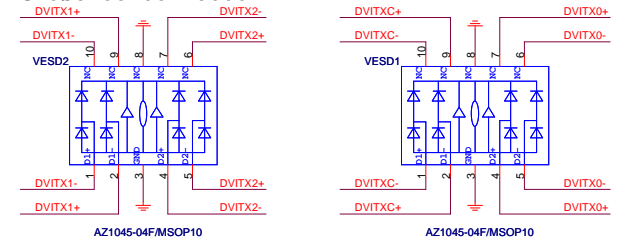
Rev: 0.73

DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%

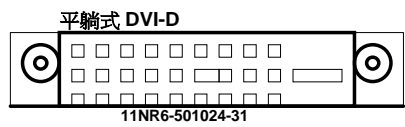


Close to connector



NET 可變

Close to connector



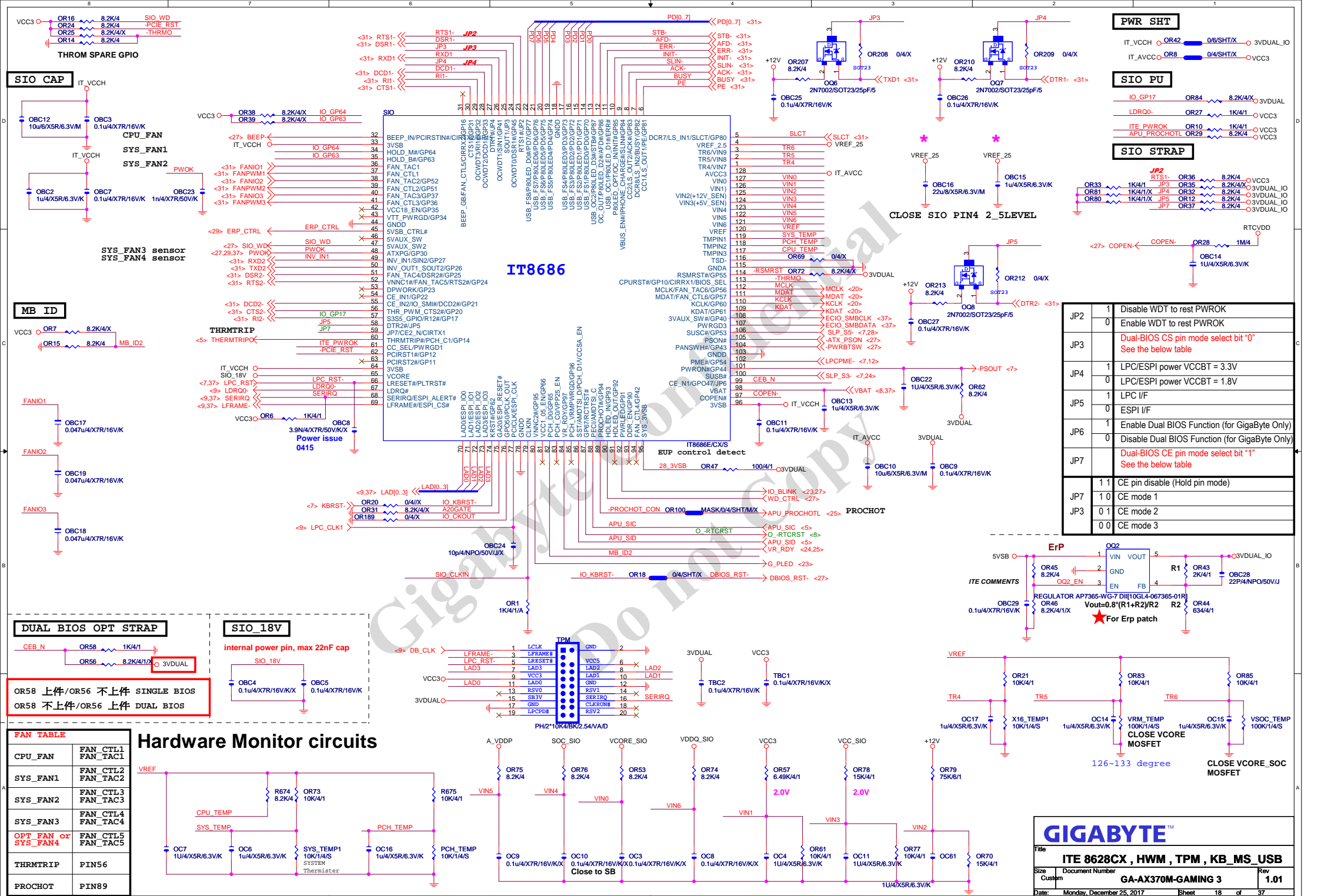
GIGABYTE

HDMI , DVI

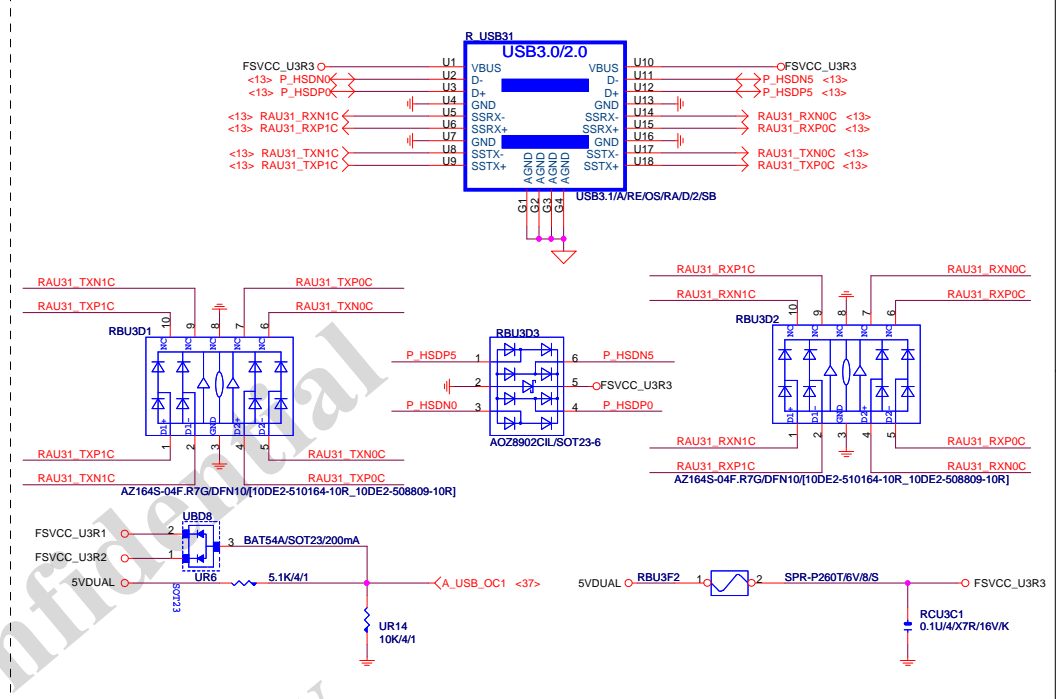
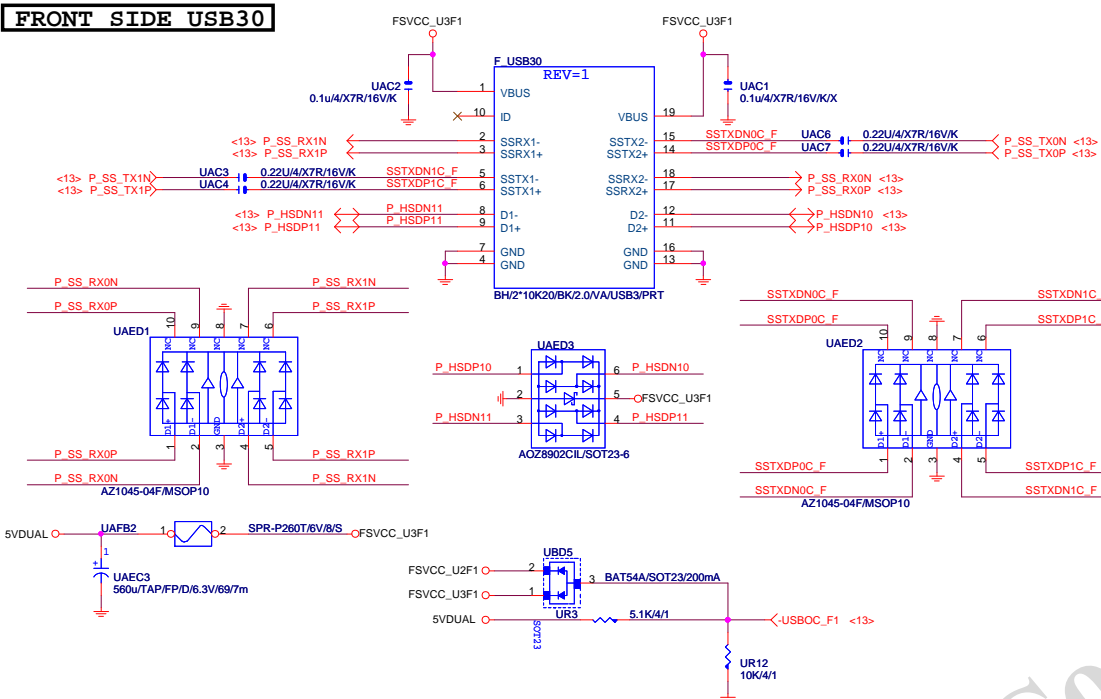
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Size: Custom
Document Number: **GA-AX370M-GAMING 3**
Rev: **1.01**

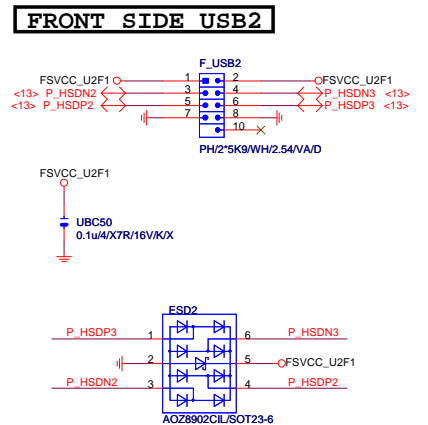
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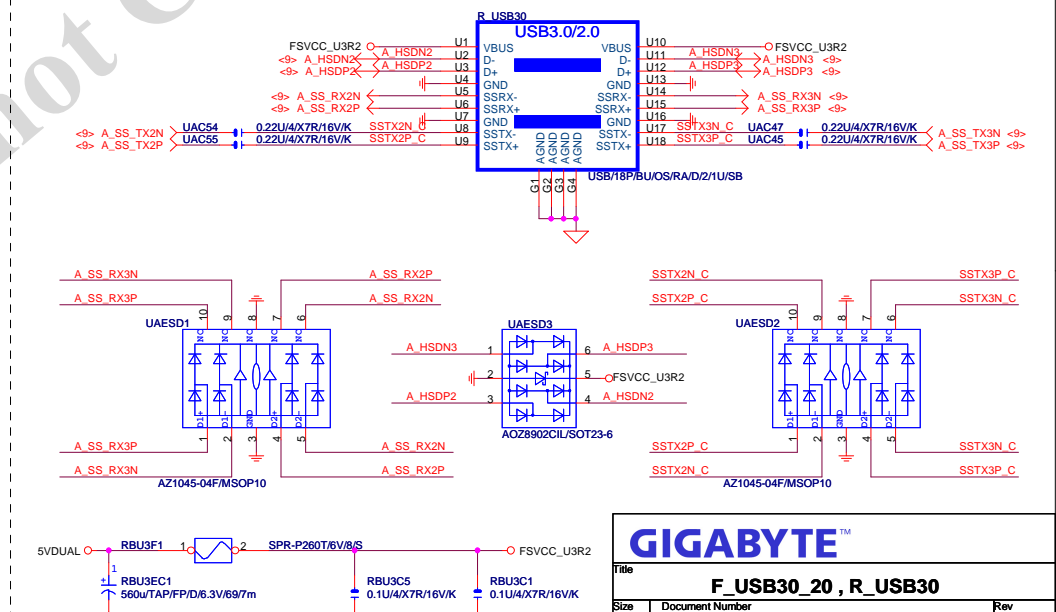
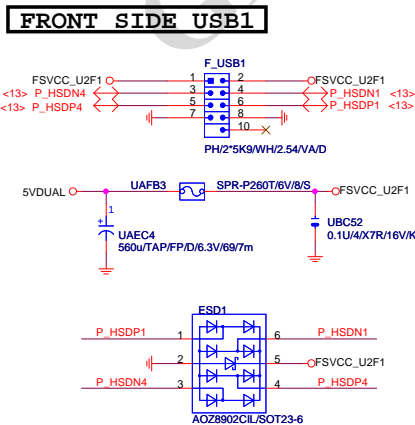
FRONT SIDE USB30

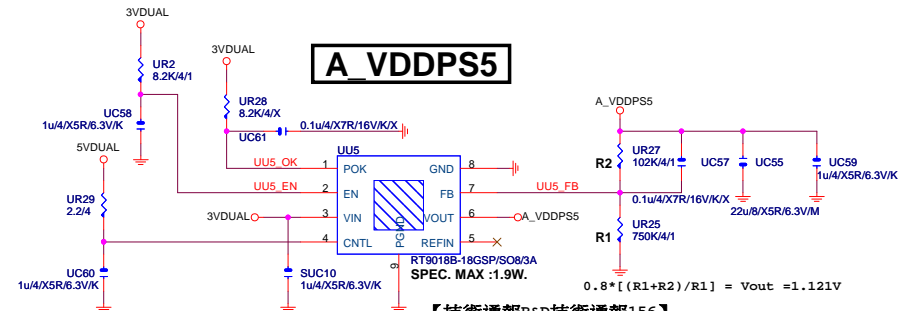
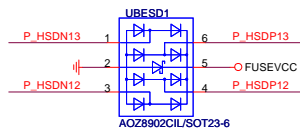


FRONT SIDE USB2



FRONT SIDE USB1



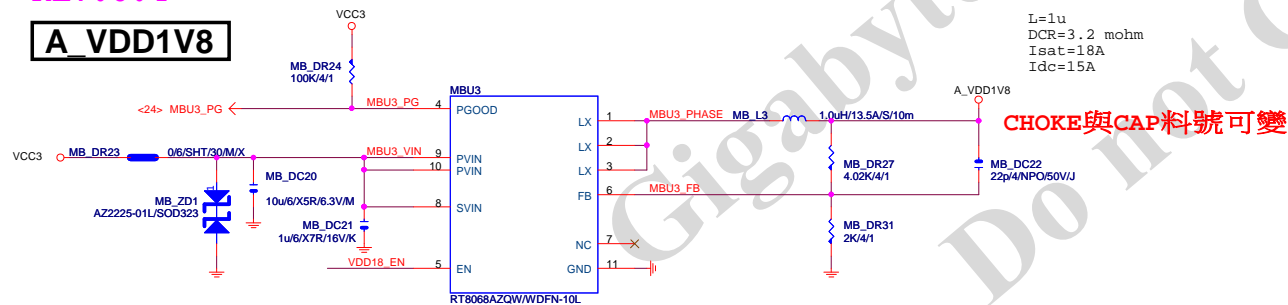


【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
(R1/R2)須做修改為100K以上電阻值

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

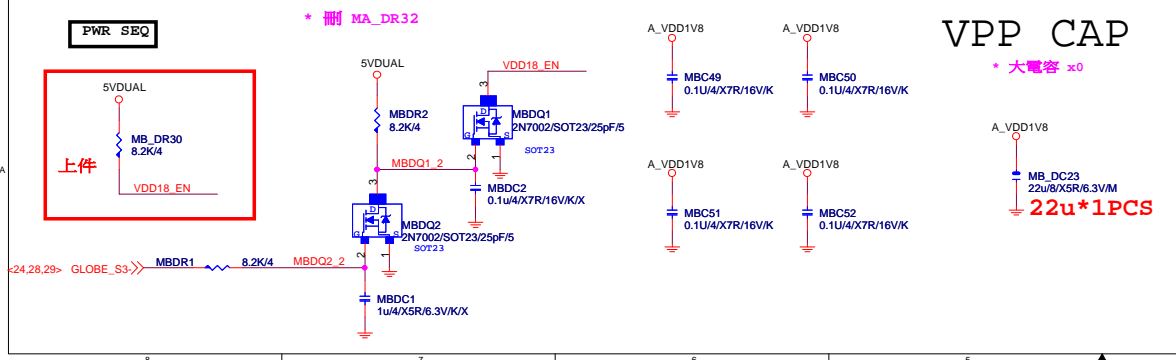
REV:0.4

A_VDD1V8



L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A

CHOKES與CAP料號可變

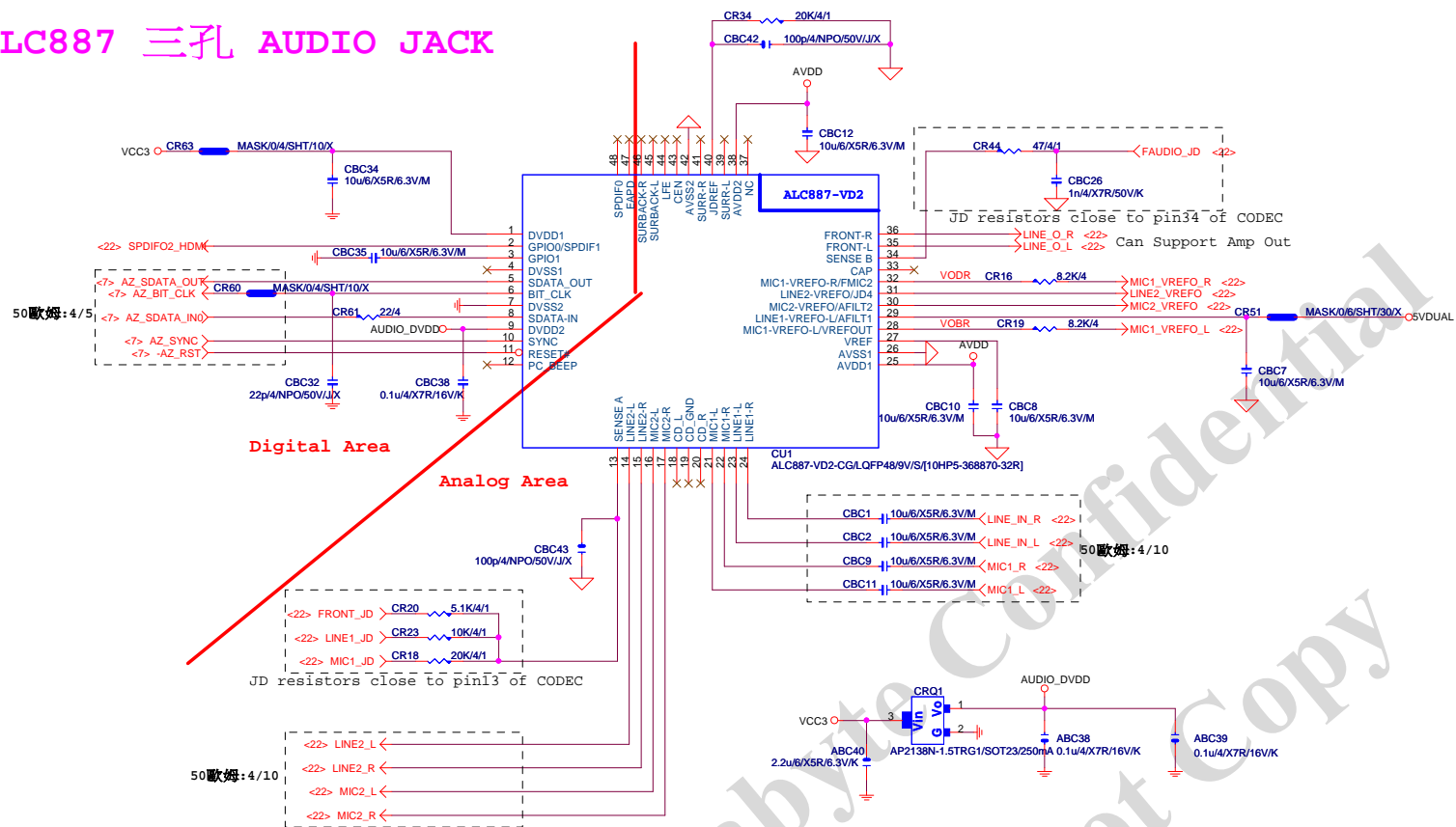


VPP CAP

* 大電容 x0

 22u*1PCS

ALC887 三孔 AUDIO JACK



LAYOUT注意:螺絲孔下GND方式
 1. MH1空間夠,下DGND
 空間不夠,改為Isolate
 2. MH2一律改為Isolate

○ MH1	MH2 ○
DGND	Isolate

LAYOUT注意:要加

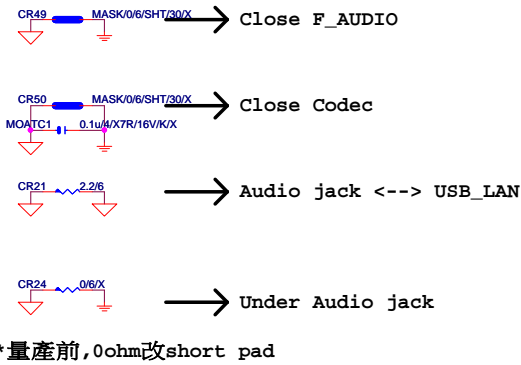
GND切割線



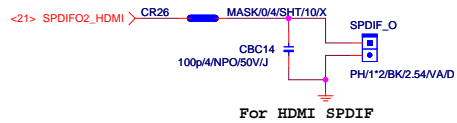
BOM OPTION : 1. Chemicon 音效電容
 2. 金屬外罩 Reserve (上件與否,依照各Model spec)
 3. LED Reserve (上件與否和LED顏色,依照各Model spec)

GIGABYTE™		
Title ALC887 CODEC		
Size	Document Number	Rev
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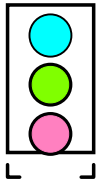


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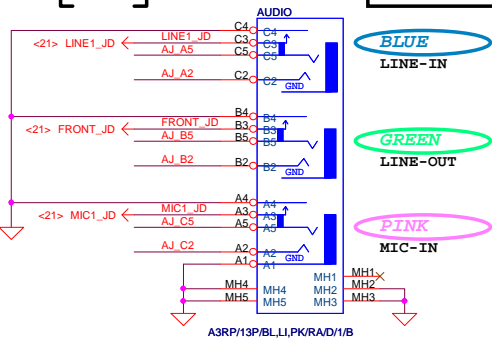


SPDIF_IN

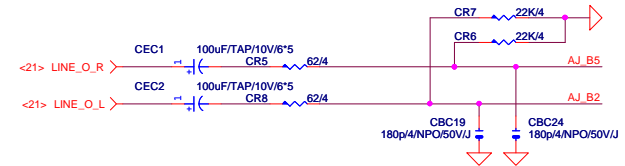
AZALIA JACK



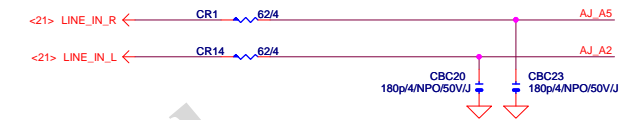
AZALIA JACK



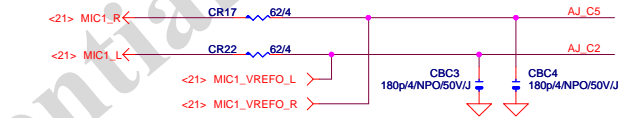
LINE-OUT



LINE-IN



MIC-IN

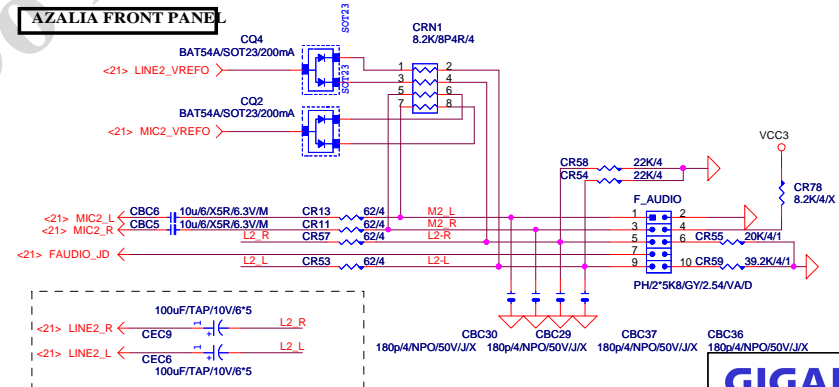


SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL

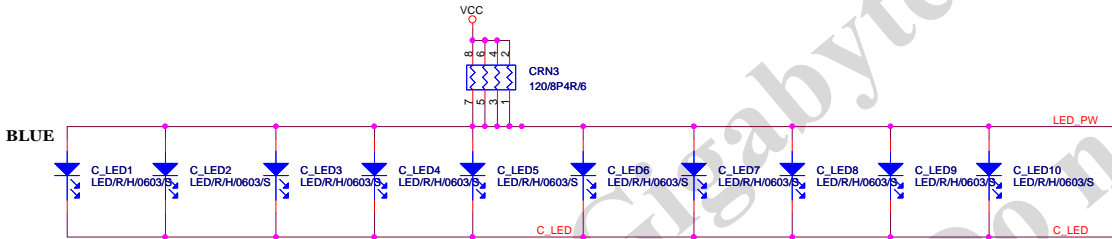


GIGABYTE™

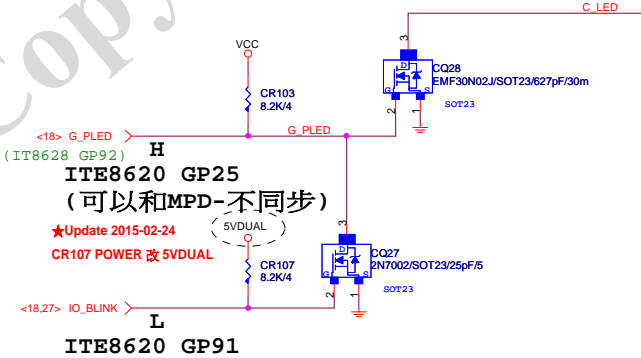
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AUDIO JACK		
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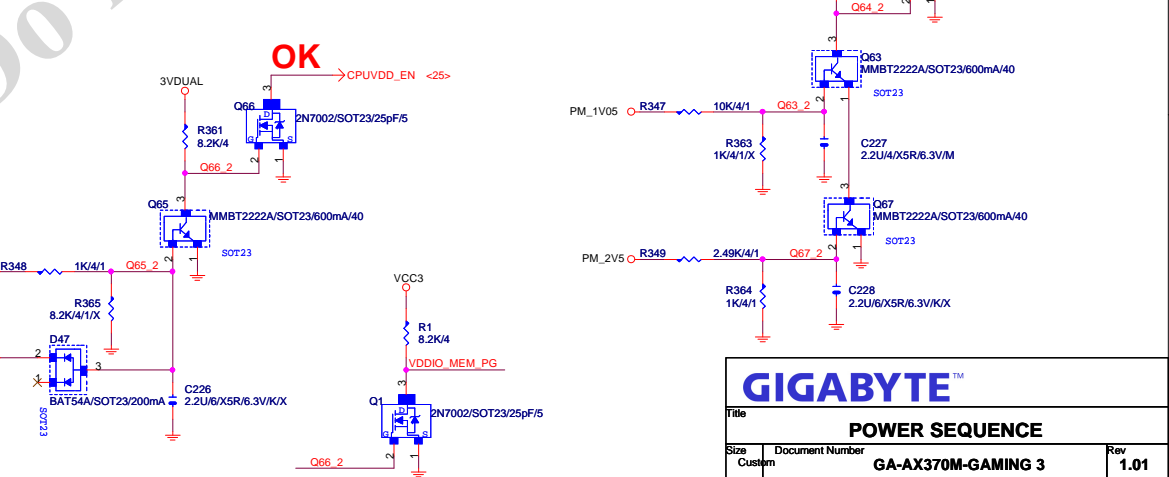
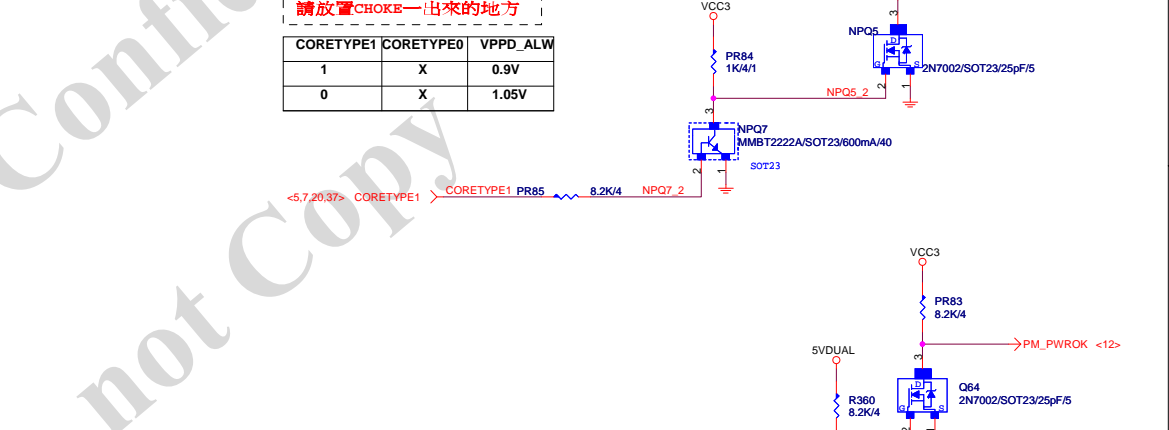
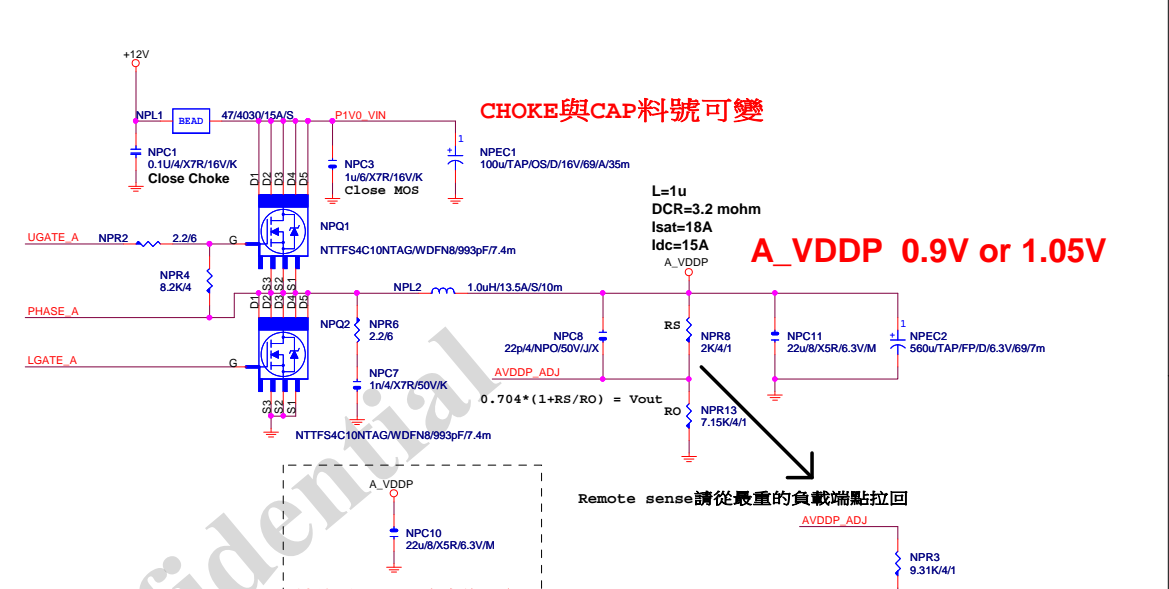
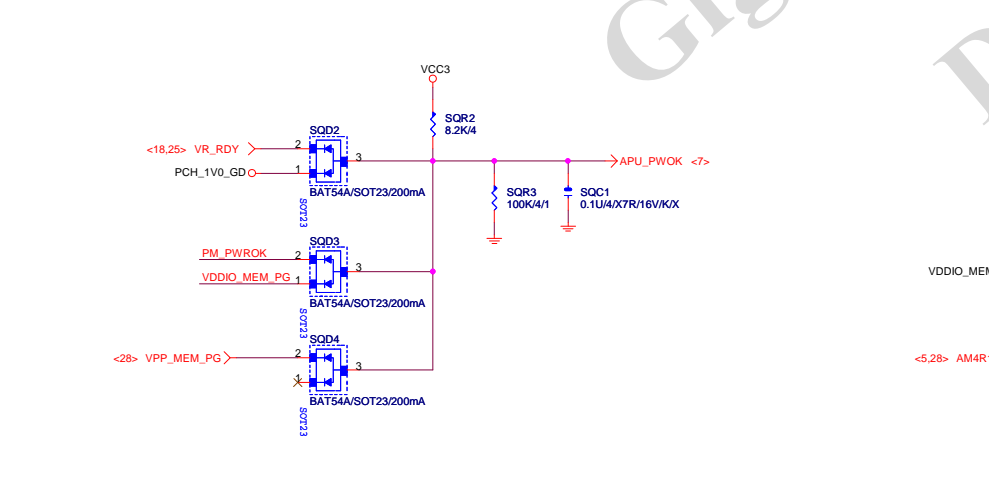
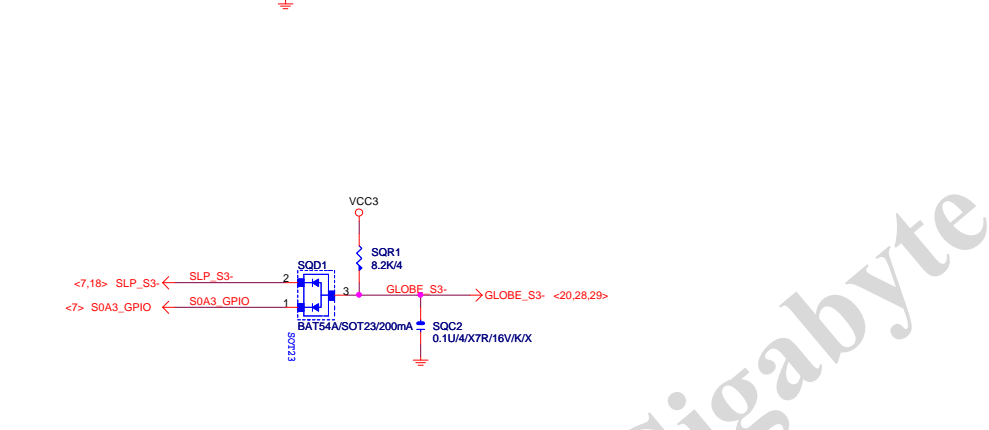
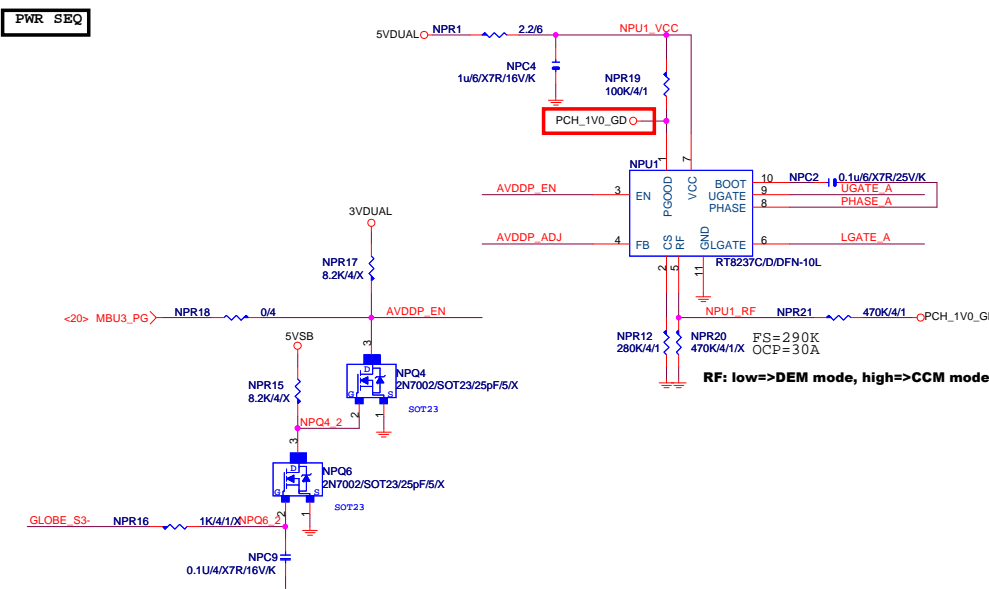
VALUE可變,LED顏色請自行修改
(預設:低亮度黃色LED:LED/Y/6/S)

	IO_GP25	IO_GP23	IO_GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L



- BOM OPTION :
- 1. Chemicon音效電容
 - 2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
 - 3. LED Reserve (上件與否和LED顏色,依照各Model spec)



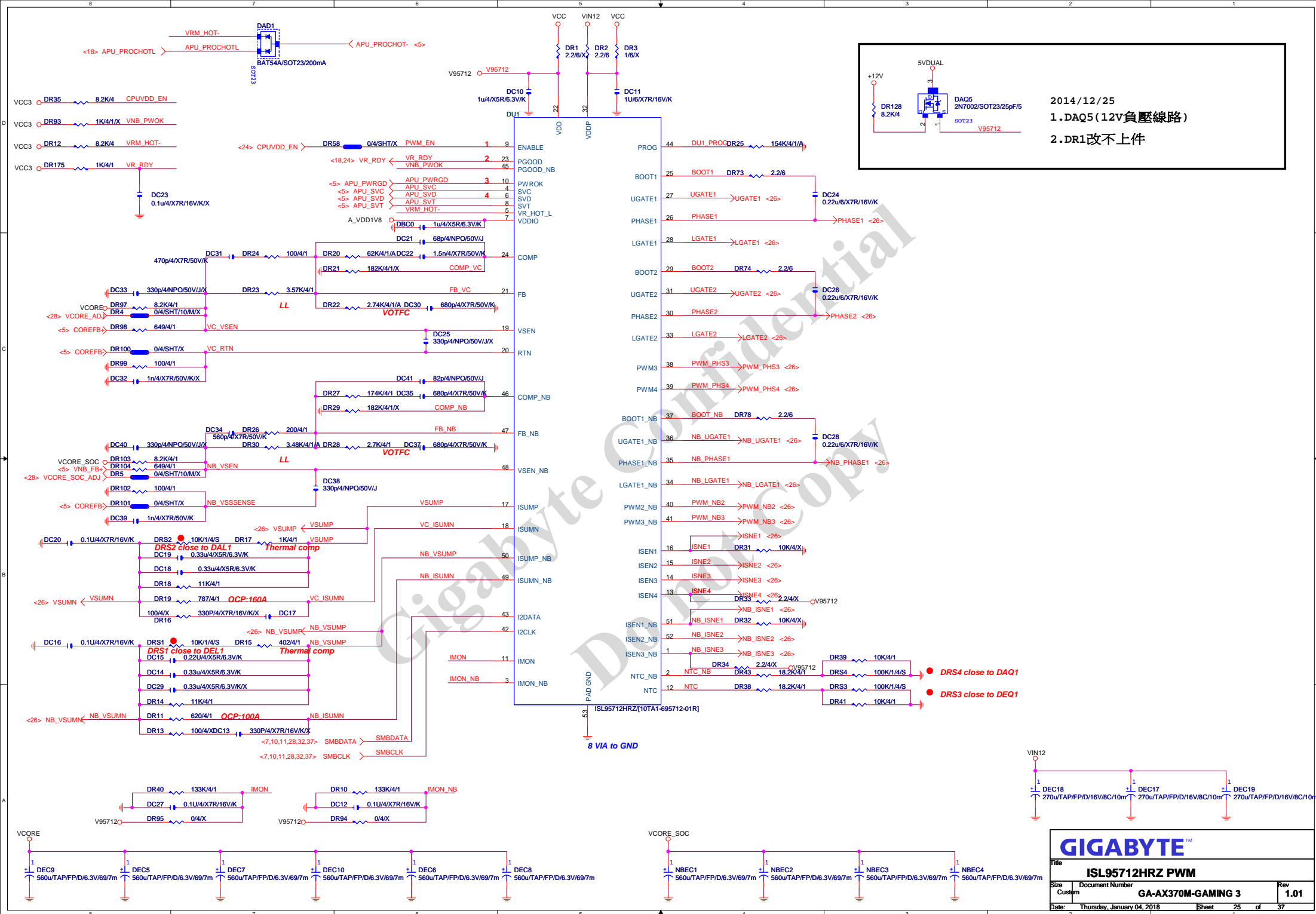


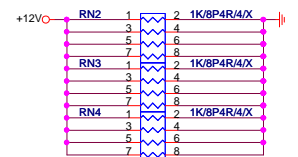
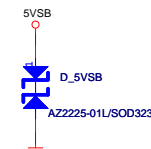
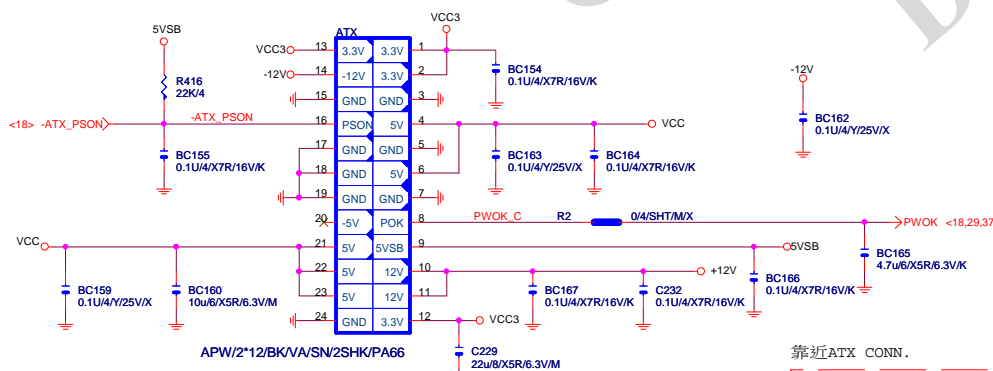
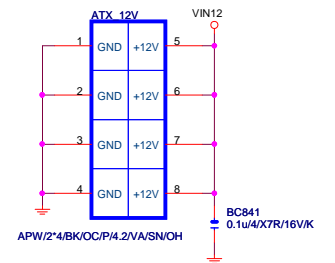
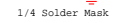
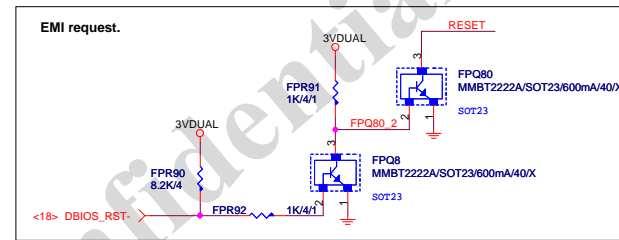
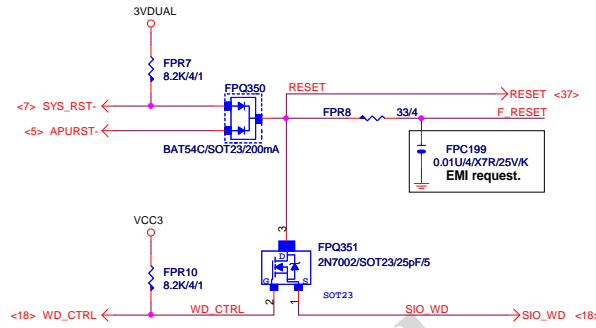
CHOKE與CAP料號可變

A_VDDP 0.9V or 1.05V

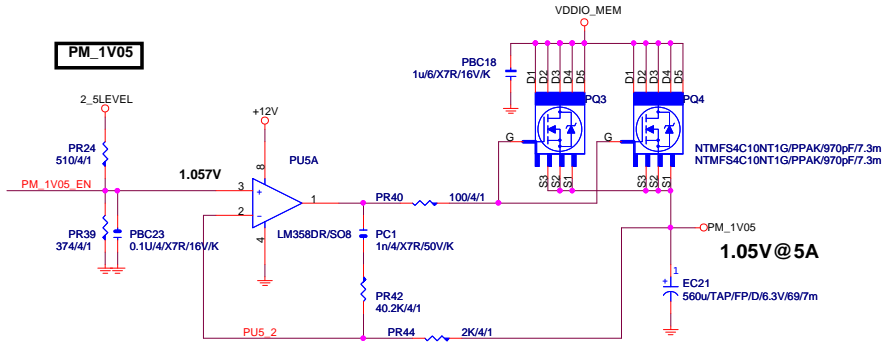
Remote sense請從最重的負載端點拉回

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

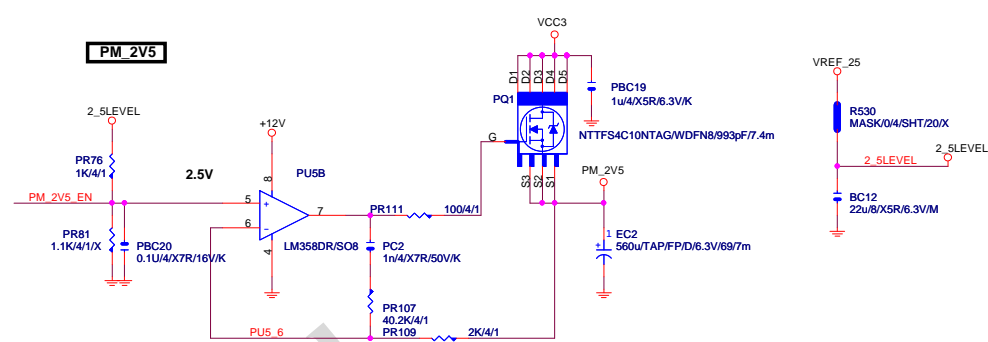




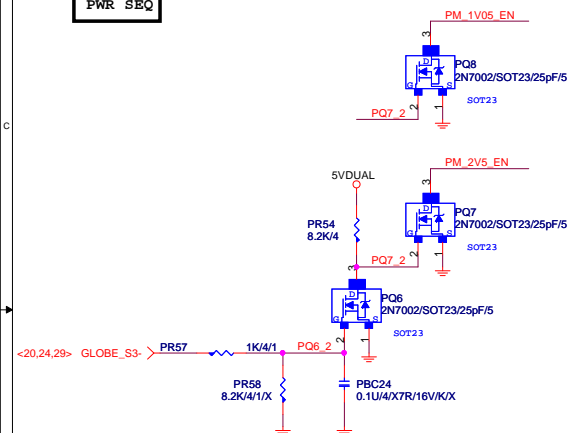
PM_1V05



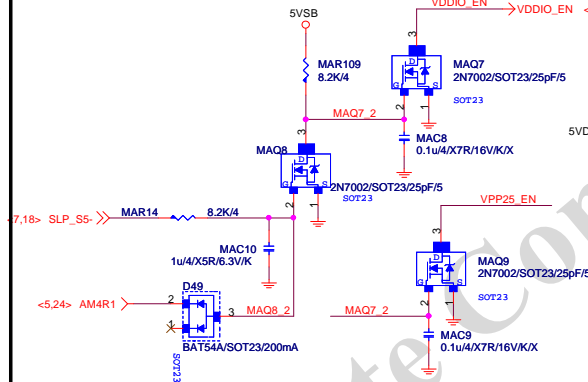
PM_2V5



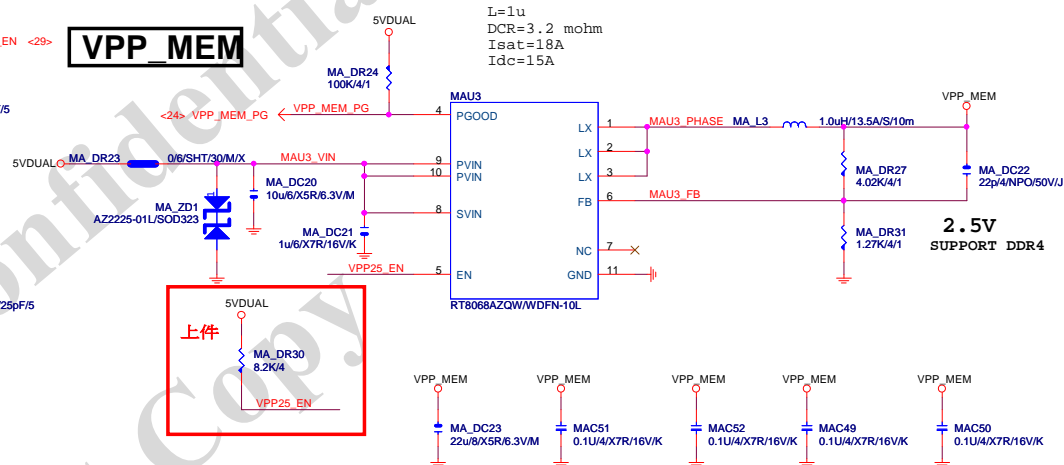
PWR_SEQ



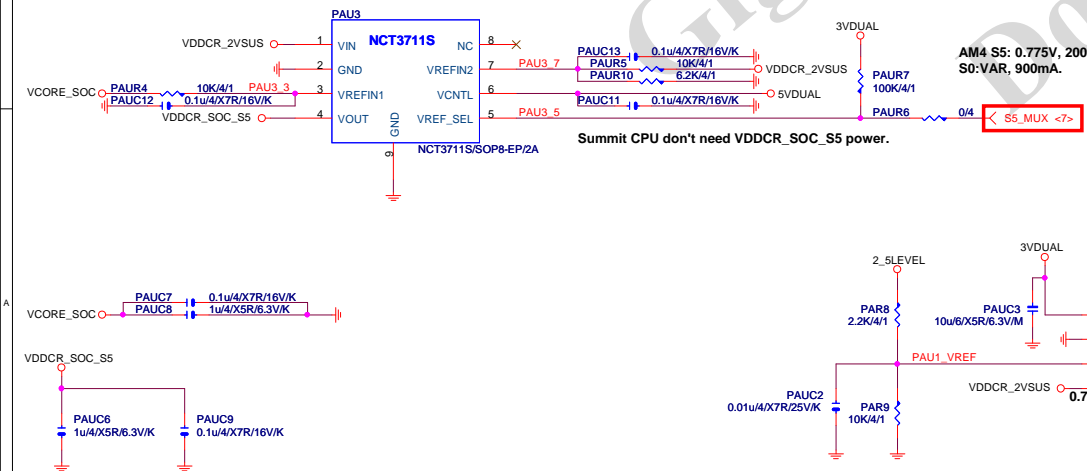
PWR_SEQ



VPP_MEM



VDDCR SOC S5

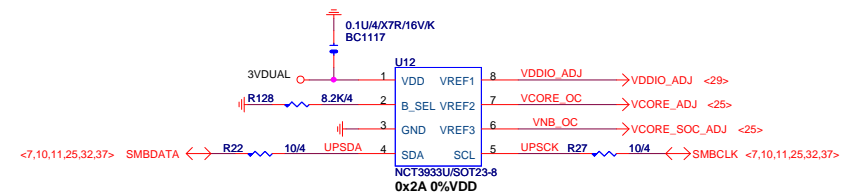


S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.

AM4 S5: 0.775V, 200mA,
S0:VAR, 900mA.

Summit CPU don't need VDDCR_SOC_S5 power.

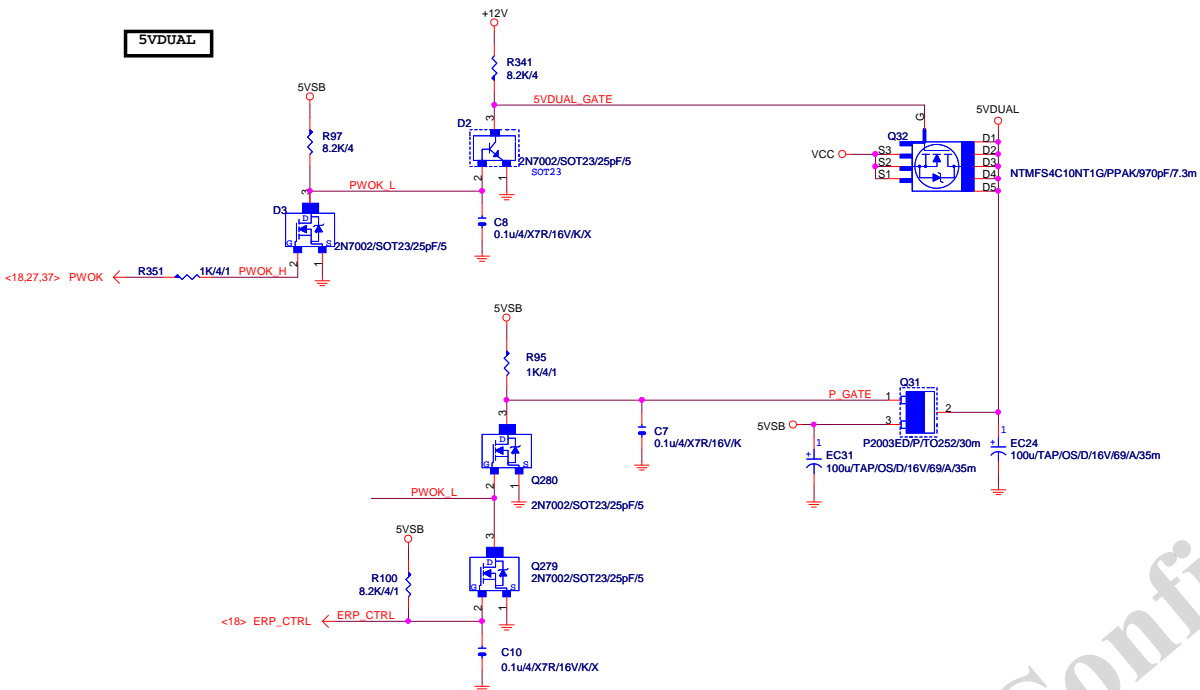
S5_MUX <7>



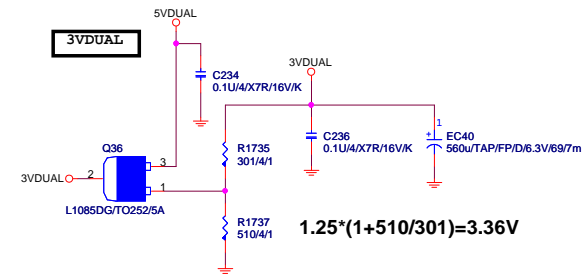
GIGABYTE

Title			
SB PWR,VDDA25,VCC11DUAL			
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5VDUAL

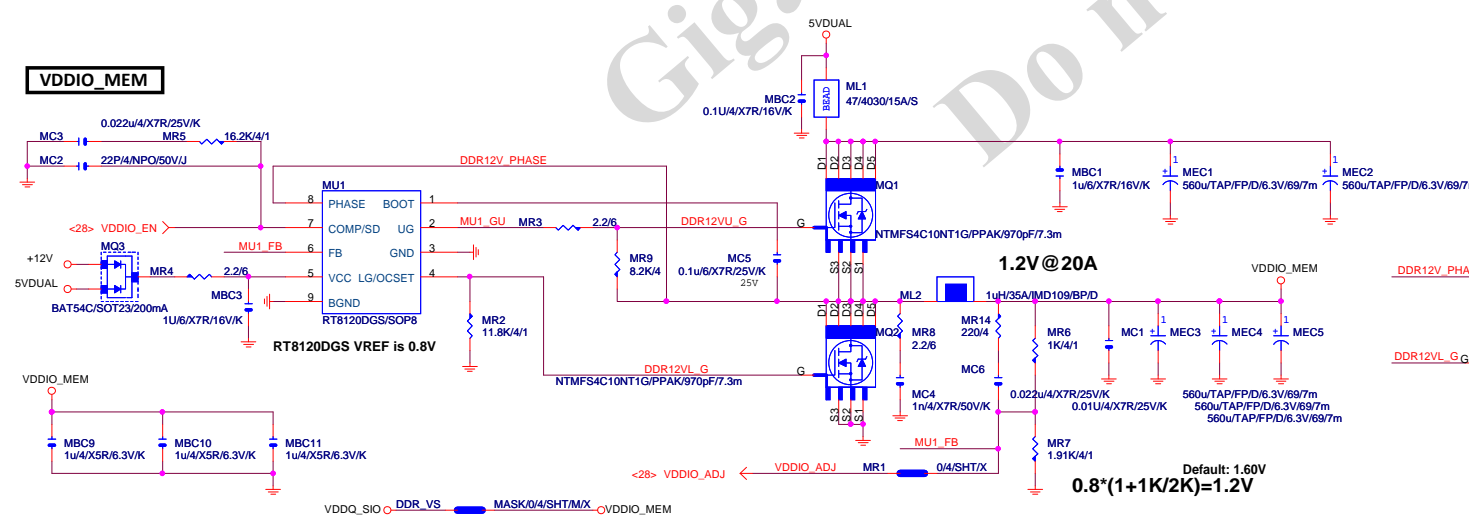


3VDUAL

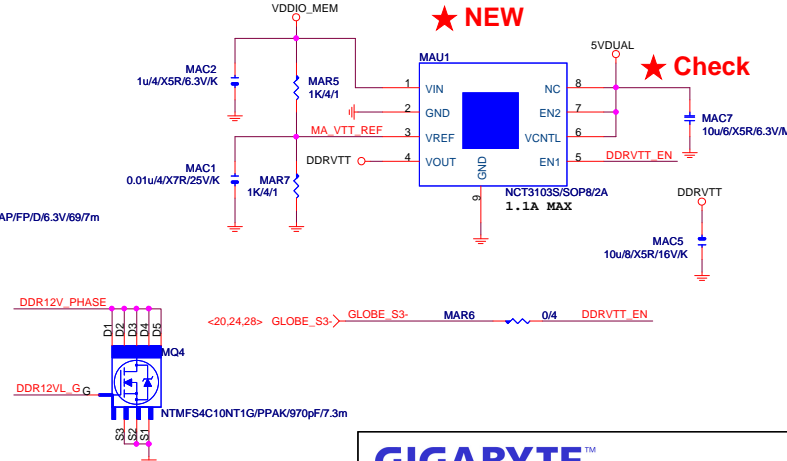


$$1.25 \times (1 + 510/301) = 3.36V$$

VDDIO_MEM

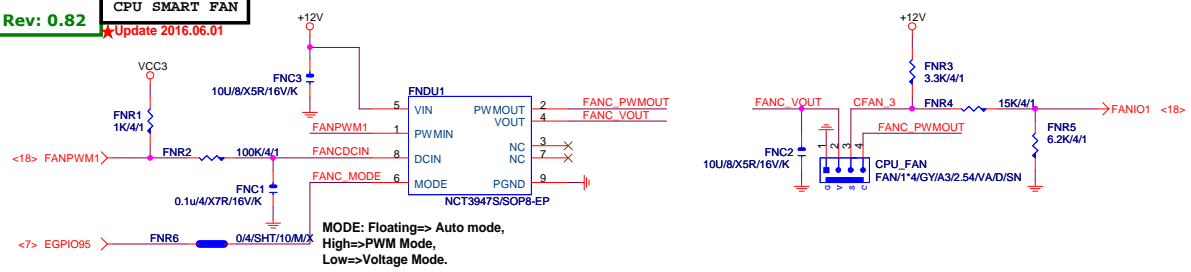


DDRVTT

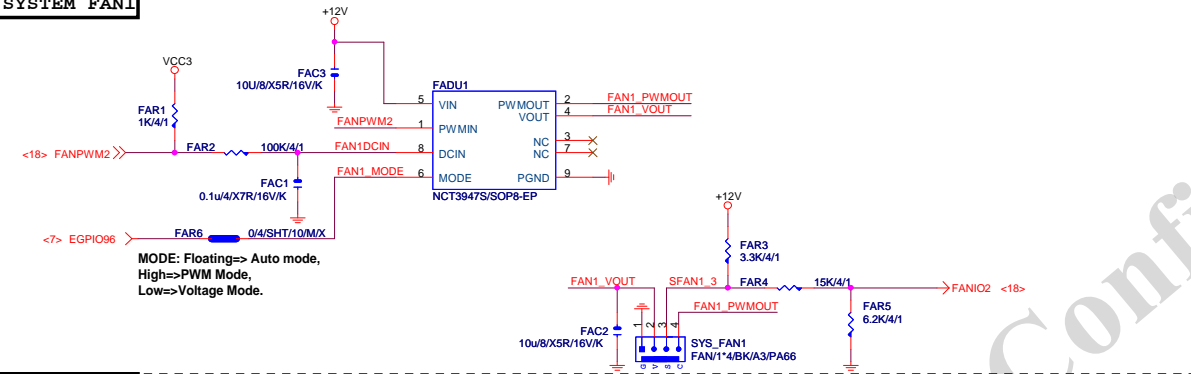


GIGABYTE

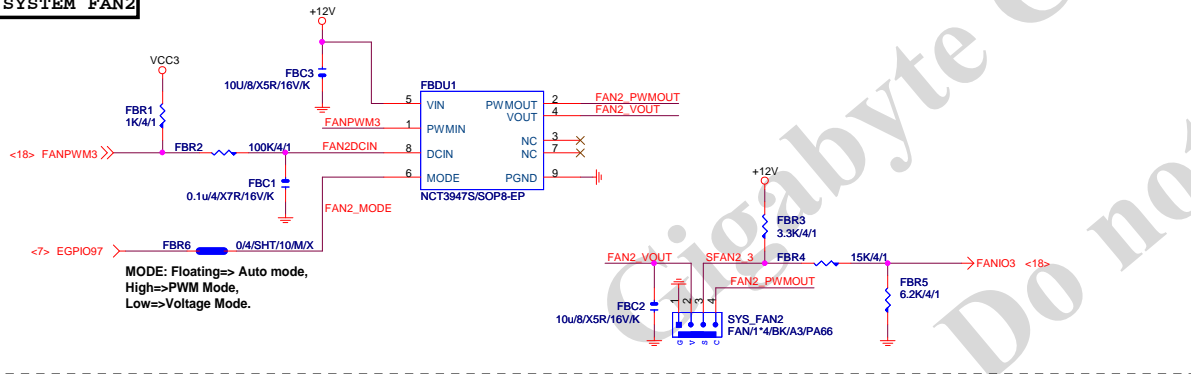
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DDR PWR, 5VDUAL, ERP		
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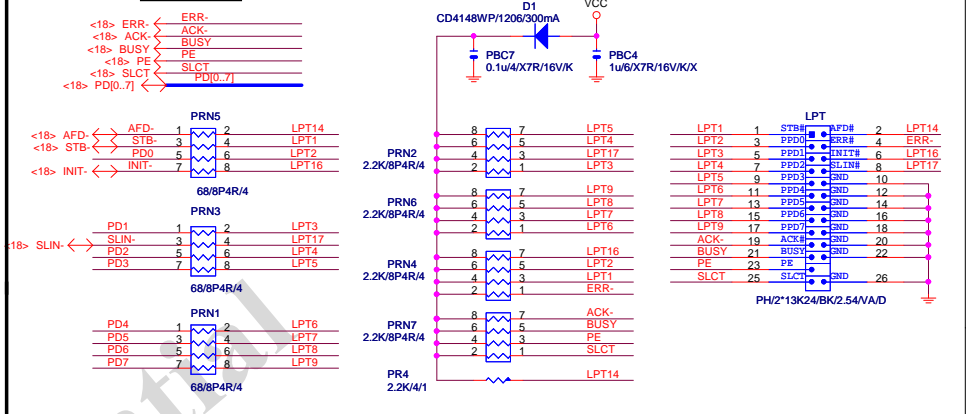
SYSTEM FAN1



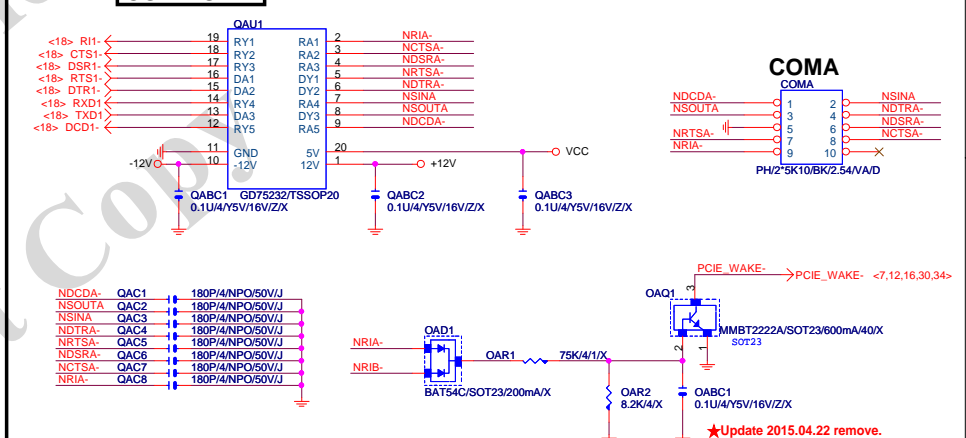
SYSTEM FAN2

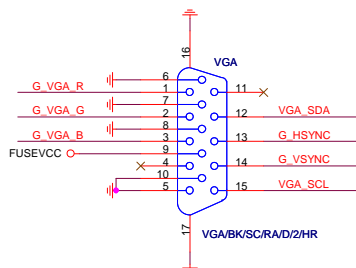
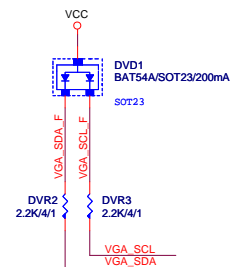
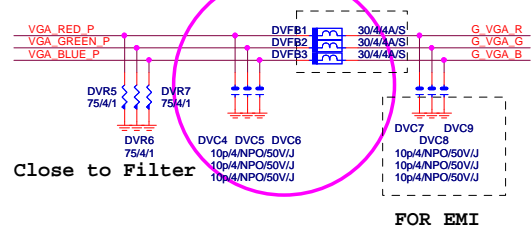
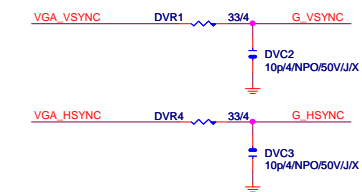
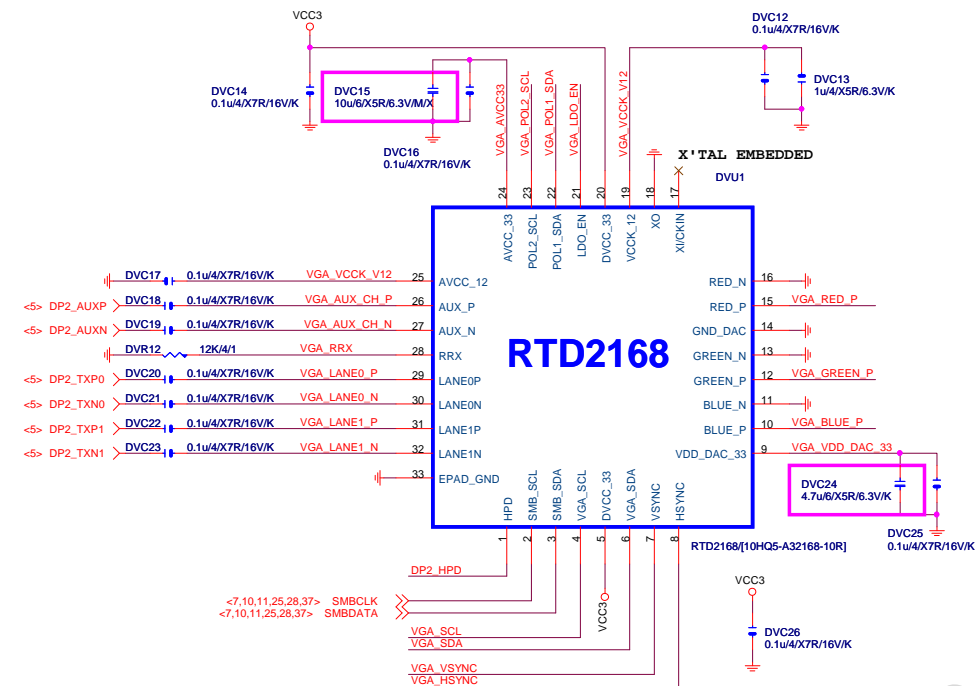


LPT PORT

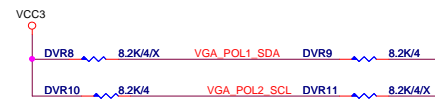


COM PORT





Power on latch



		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO

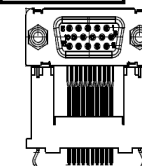
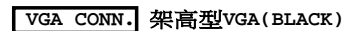
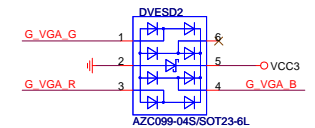
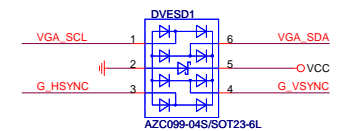


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

DP HPD



Gigabyte Technology



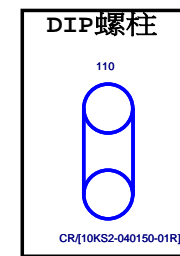
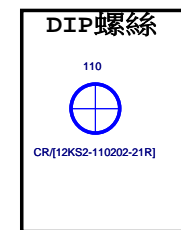
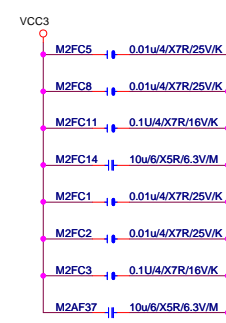
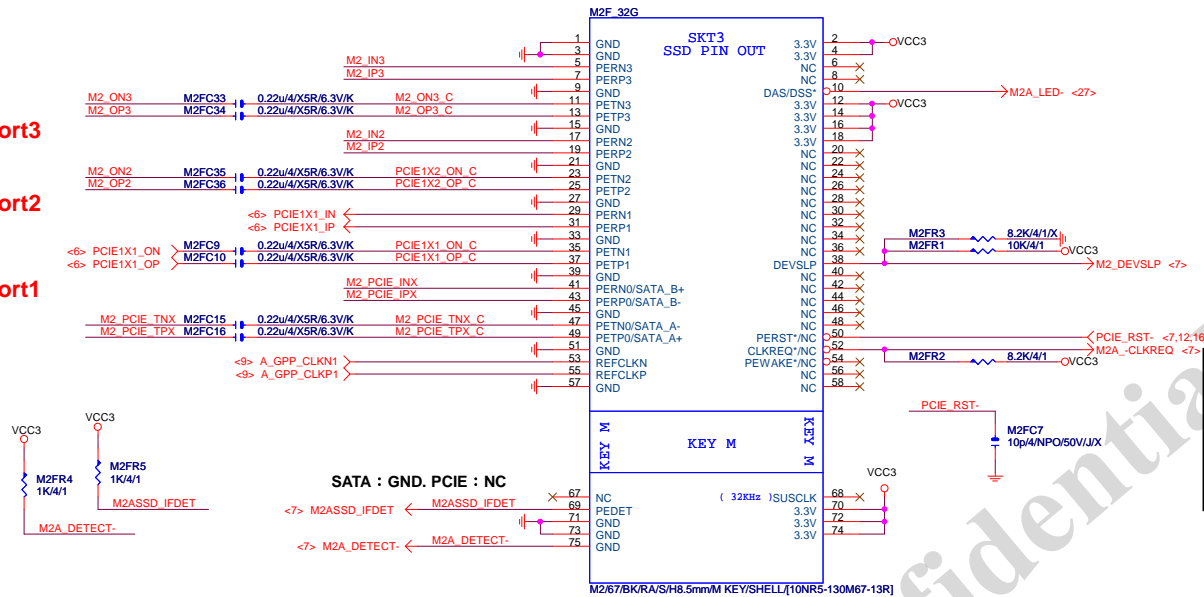
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M.2 Lane4 from AM4 port3

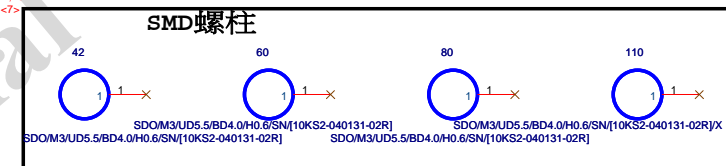
M.2 Lane4 from AM4 port2

M.2 Lane4 from AM4 port1

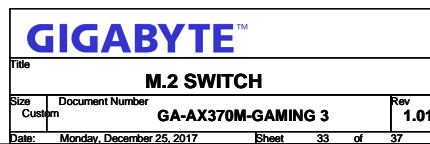
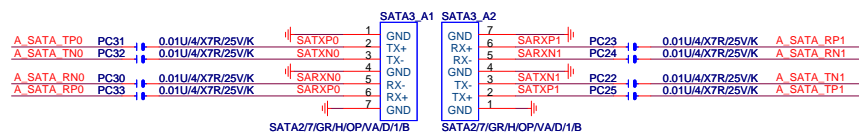
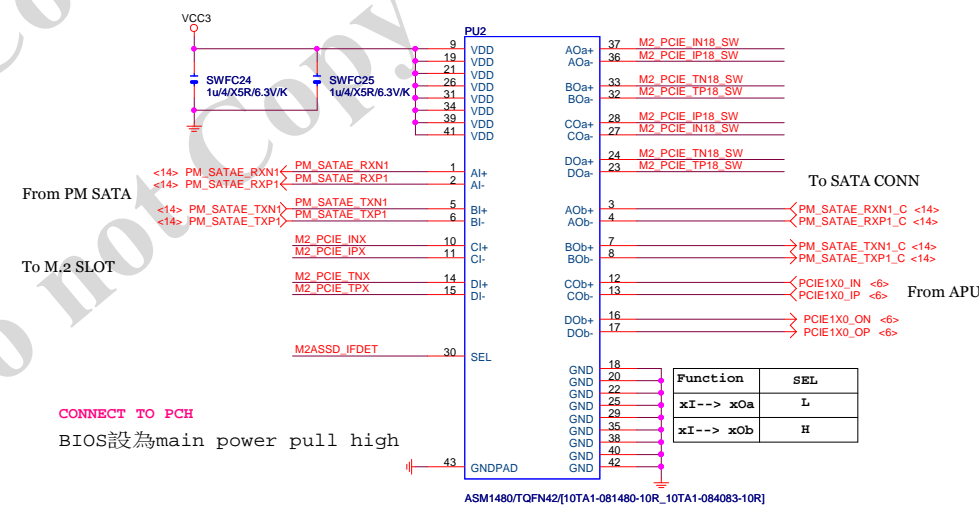
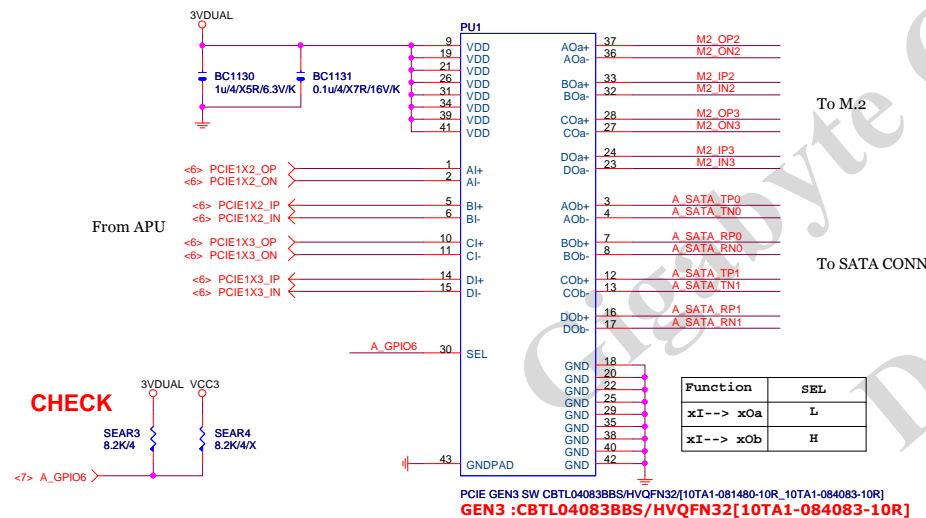
by SWITCH Select

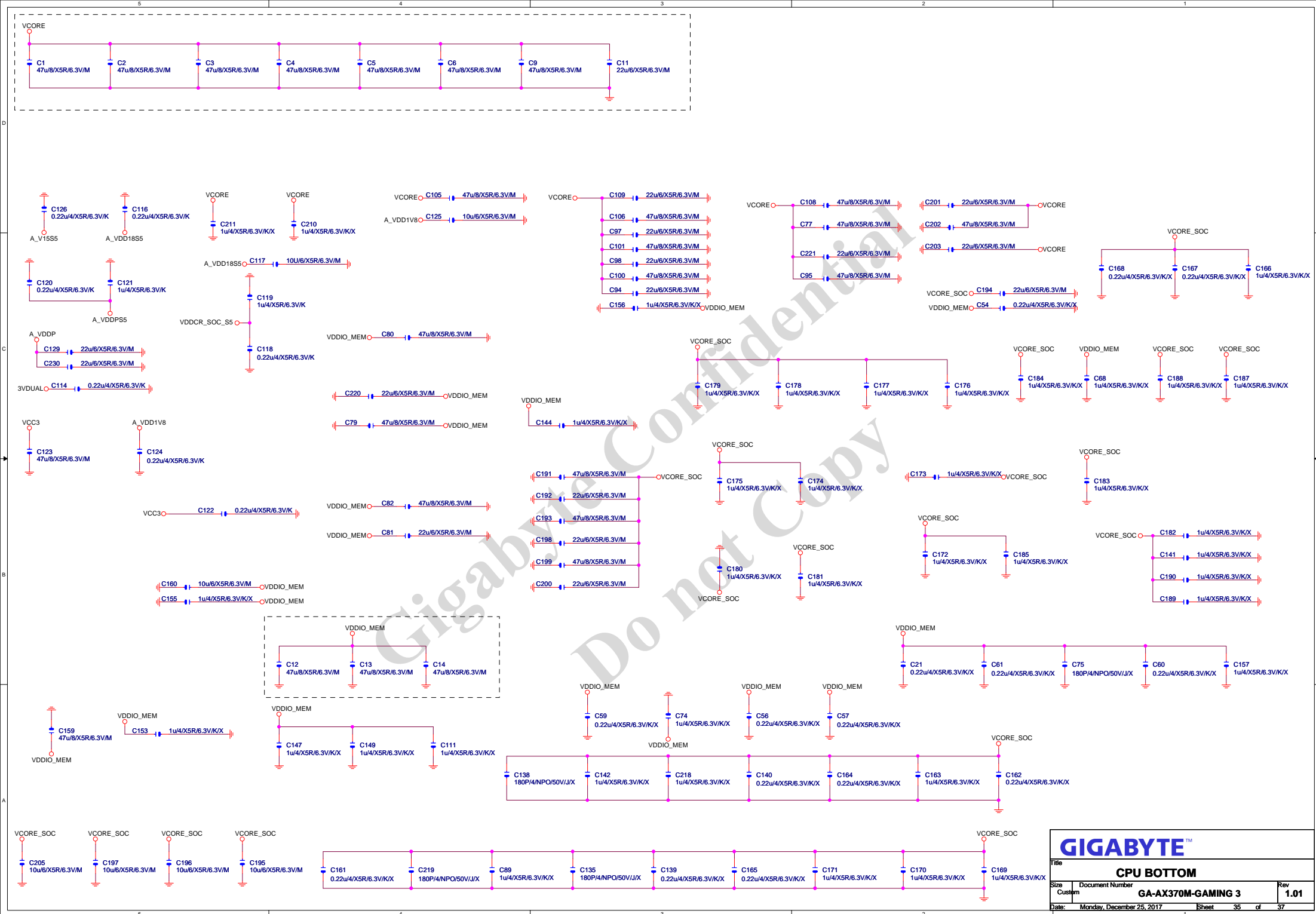


架高

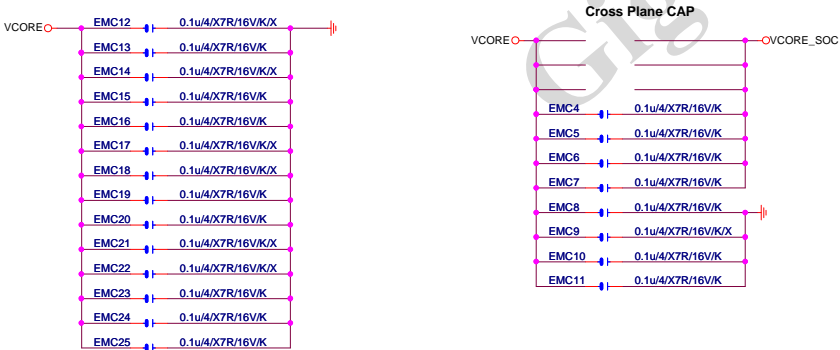


M2F_32G
M2F_32G/[12SP1-S10205-02R
 **M2 HEATSINK**





CPU TOP CAVITY



GIGABYTE™

Title			
CPU TOP			
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